Compensation of Voltage Disturbances and Downstream Fault Currents Reduction by Using a New Topology of DVR-FCL

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Abstract:

The growing rate of energy consumption is a reason for establishment of new power plants which leads to increment in fault current level. One of the solutions to overcome this problem is utilization of fault current limiters (FCLs). Another concerning issue in energy generation is the satisfactory voltage quality in grid and to deal with it, a power electronic based device, known as dynamics voltage restorer (DVR), is introduced. However, in power grids FCL and DVR are independent devices. In this paper, a novel topology is proposed which linking DVR and FCL, provides substantial benefits. According to grid state, the DVR-FCL has four operating modes. Moreover, for appropriate operation of the presented topology, a suitable control method is proposed. The DVR-FCL and the control method are verified considering the simulation results.

Keywords: DVR; FCL; voltage disturbances; downstream fault current

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1. Introduction

Nowadays most of residual, commercial and industrial users (especially automated industrial processes) are sensitive to power quality problems [1-3, 6, 21-24]. Voltage quality is one of the well-known power quality problems and voltage sag is the most common and sever incident which is defined as a short voltage reduction from 0.9 p.u. to 0.1 p.u. of nominal voltage. It usually happens because of remote faults or start of large loads [1-6, 8, 23]. Even if voltage sag lasts only for few cycles, it can disrupt sensitive loads or cause malfunction which results in huge financial losses. Because of the problems mentioned above, this issue has drawn remarkable interest [1, 4,5, 7,8, 22]. A solution to handle this problem is the increment of the tolerance margin in equipment which evidently leads to more cost. Another key answer is utilization of dynamic voltage restorer (DVR). DVR is a power electronic based instrument which is capable of injection of voltage series to network in controllable magnitude, frequency and phase angle. From the energy storage viewpoint, DVR is classified in two types [1]. The stored energy to compensate load voltage contains energy storage systems such as batteries, capacitors, flywheel or SMES [1, 9]. However, the other type does not use considerable energy storage system and takes its energy from the grid [1, 10].

Fig. 1 shows basic DVR topology. According to this Figure, it is obvious that, conventional DVR is composed of a DC voltage source, H-bridge voltage source inverter (VSI), second order filter, bypass switches and injection transformer [2, 11, 23].

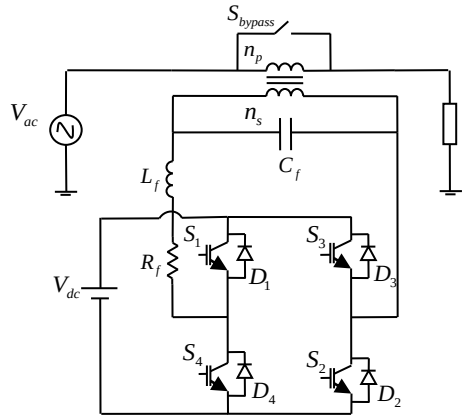


Fig. 1. Conventional DVR topology

At the moment, the growing request for electric power causes increment in electric power generation which results in establishment of new power plant, transmission and distribution systems. Nevertheless, in this case, the fault current level becomes seriously greater than tolerable current rating of apparatuses and protective components. This occurrence can be managed at least by three solutions: 1) Installation of new circuit breakers with higher current rating in substation. 2) Changing power system configuration (bus splitting) to lessen available fault current amplitude. 3) Utilization of devices restricting fault current to permissible value. The first and the second suggestions need great financial support. Moreover, in the second one, specific benefits owing to the system configuration are lost. As a result significant emphasis is put on studying the fault current limiting apparatus which is more cost effective than the first solution and yet power system configuration does not need to be reformed [12-15].

In [12], solid state fault current limiter is categorized in three following classes; the series switch, the bridge and the resonant. In the normal state of the network, all of the fault current limiters (FCL) maintain low impedance so that power flow is not prevented. On the other hand, at the fault occasion, FCL impedance rises rapidly.

As mentioned before, one class of FCLs is the bridge type with the basic configuration exhibited in Fig. 2 .This FCL is composed of H-bridge rectifying part, DC reactor and DC voltage source. In normal state, all diodes are in full conduction mode and in the case of short circuit fault occurrence, D_1 and D_4 or D_2 and D_3 diode pairs conduct in positive and negative half cycles, respectively [12, 15].

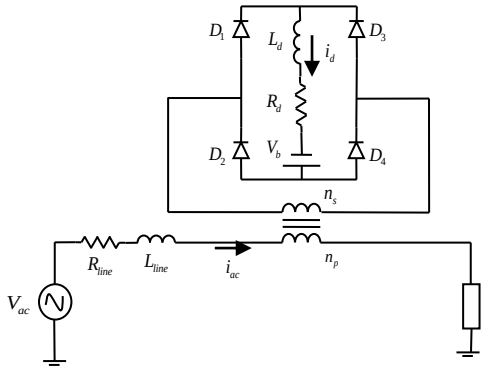


Fig. 2. Conventional bridge type FCL

Multifunction DVRs, holding almost identical principals, are investigated, though [7, 16-19, 23]. When voltage fault arises, DVR performs as voltage restoring device and compensates voltage sag or swell but when current fault occurs, its control strategy changes and operates as FCL. All of above-mentioned DVRs operate as either voltage restorers or fault current limiters. So if each of transistors in inverter faces any defect, proposed system neither perform as a DVR nor as FCL. This is the principal motivation point of this research. To overcome the aforementioned limitation, this paper proposes a new topology and its related control method. According to the state of the

grid, this topology is capable of performing as FCL or DVR. The proposed topology has some economic advantages such as reduction in the number of the used diodes, transformers and etc. This letter is organized as follow: In section II, III, and IV the topology, its control method, and the analytical study of the DVR-FCL are explained, respectively. Section V contains the performance of the topology. In section VI, the achieved advantages are depicted. Then, in section VII, applicable simulation in the PSCAD/EMTDC software [25] is demonstrated and in the last section, contribution of this paper is presented.

2. Proposed Topology for Single Phase

Fig. 3 shows the new topology proposed for single phase DVR-FCL. It consists of a bridge type FCL and a DVR. The FCL mentioned in the proposed topology includes rectifying part, DC reactor, series DC biased voltage source, freewheeling diode and current fault detection switch. In addition, DVR is composed of DC voltage source, VSI (H-bridge), second order filter and voltage fault detection switch. The proposed topology is connected to the grid by means of a transformer with $a=\frac{n_s}{n_p}$ turns ratio. The DC voltage source for DVR and FCL can be supplied by rectifiers that are connected to the network.

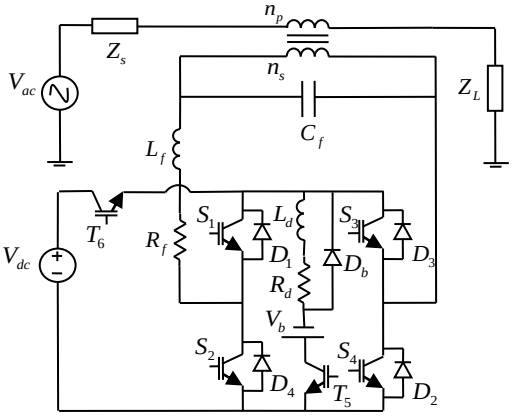


Fig. 3. Proposed DVR-FCL

3. Analytical Study of Proposed DVR-FCL

Analytical study of the DVR-FCL is same as the separated DVR and FCL, which brings simplicity. The only difference is about FCL operating mode. In other words, the output filter of the DVR causes voltage drop across it, which is not exist in the case of single FCL (Fig. 2). However, because of small value of the mentioned voltage drop, it is practical to ignore it.

According to Fig. 2, the differential equation of the DC reactor current in the ideal form can be written as follow.

$$L_d \frac{di_d}{dt} + R_d i_d - V_b = 0 \tag{1}$$

where L_d, R_d, V_b, and i_d represent inductance of reactor, resistance of reactor, series DC voltage source, and reactor current, respectively. Considering zero initial state for i_d, (1) can be solved as follow.

$$i_d = \frac{V_b}{R_d}\left(1 - e^{-\frac{R_d}{L_d}t}\right) \tag{2}$$

$$I_d = \frac{V_b}{R_d} \tag{3}$$

where I_d is the steady state value of i_d. According to Fig. 2, following equations can be written for diodes current.

$$i_{D_1} + i_{D_3} = i_d \tag{4}$$

$$i_{D_2} + i_{D_4} = i_d \tag{5}$$

$$i_{D_4} + i_2 = i_{D_1} \tag{6}$$

$$i_{D_3} + i_2 = i_{D_4} \tag{7}$$

where i_{D_1}, i_{D_2}, i_{D_3}, i_{D_4}, and i_2 are representing, D_1, D_2, D_3, D_4, and secondary of injection transformer currents, respectively. Also according to Fig. 2, it is obvious that D_1 and D_2 pair and D_3 and D_4 pair are in the same condition. In other words, current passing through the mentioned pairs are equal. Therefore, according to (4)-(7) and given explanation, the current of diodes may be expressed as follow.

$$i_{D_1} = i_{D_2} = \frac{1}{2}(i_2 + i_d) \tag{8}$$

$$i_{D_3} = i_{D_4} = \frac{1}{2}(-i_2 + i_d) \tag{9}$$

According to (3), (8), and (9), in the normal state of the grid, V_b is chosen in a way that $|i_2| < i_d$. Therefore, four diodes will conduct in the normal state, simultaneously. Occurrence of current fault, cause significant rise in $|i_2|$. Considering (8) and (9), a single pair of diodes will conduct in the positive and negative period of the current, which will be discussed in the following sections.

{R3-5} It is important to note that, some of the presented topologies for the FCL do not utilize V_b.

However, in the mentioned cases, during normal operation, the FCL would be charged and discharged, every cycle. Therefore, considerable voltage drop appears on the FCL. As the paper is concerned with the improvement of the power quality issue (compensation of voltage fault and limitation of current fault), V_b is applied to the proposed DVR-FCL [28-29].

The main challenge in the design of the proposed topology is the accurate determination of V_b, L_d, and R_d.

L_d is chosen according to the economical aspect. In other words, if very small reactor is chosen, the reactor current could rise to the high value rapidly. Then, the stored energy in the reactor becomes high, too. On the other hand, if large value for the reactor is chosen, proper limitation of the fault current will be achieved. But the fact remains that, the stored energy in the reactor is still high. Therefore, the reactor value has to be chosen in order to minimize the stored energy. Also, according to the size of the reactor (turns number, diameter of wire, etc) R_d can be calculated. In order to minimize the ohmic loss in the FCL, the reactor is designed in a way that minimizes R_d.

As mentioned before, V_b is chosen according to the line current and (3). In other words, if the steady state value of the reactor current is considered to be five times larger than the maximum value of line current, in accordance with (3), V_b can be calculated [15].

4. Proposed Control Method

In order to illustrate control method in detail, it is divided into three subsections. In the first subsection, voltage fault existence is detected. When fault type determination is accomplished, according to the network state and the discovered fault type, FCL or DVR portion of the proposed topology is enabled. In the second part of the control method, the reference voltage is generated as DVR is launched. In the third part, according to the generated reference voltages, the off and the on time intervals for the switches are calculated and respective commands are sent. The described procedure is clarified in details in the following.

4.1. DVR or FCL Operation Determination

As mentioned previously, this step is the first stage of the control method which determines the operating part of the proposed DVR-FCL online. It checks current or voltage fault occurrence conditions. So if the RMS value of line current exceeds the reference current, current fault is detected and subsequently, T_5 is turned on. Also when the grid is in the normal state, T_5 is maintained on. But, if a voltage fault such as voltage sag happens, T_6 is turned on and DVR restores load voltage. Fig. 4 shows this part of the control method.

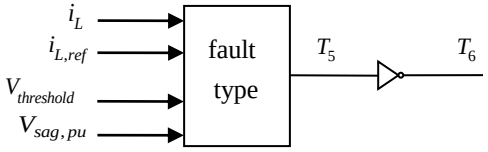


Fig. 4. Fault type detection

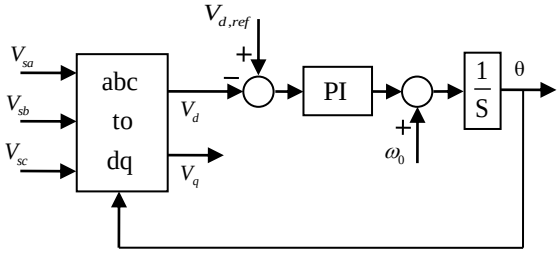


Fig. 5. Typical PLL structure

4.2. Reference Voltage Generation

Fig. 6 shows the control block diagram of the proposed DVR-FCL. As this Figure shows, the grid voltage is transformed to dq synchronous reference frame using the phase angle output of phase-locked loop (PLL). Fig. 5 shows the typical structure of the PLL [27]. The PLL function is based on the synchronism between the source voltage and the dq reference frame frequency. Indeed, in the normal condition the PLL follows the phase angle of the source voltage, continuously. The PLL output phase angle is frozen by voltage fault occurrence. In other words, if the phase jump has been occurred during voltage fault the system would have been able to detect it. Then, according to the preferred control method (pre-sag method, minimum energy method, and minimum voltage method) the desired phase angle advancement in the injected voltage is achievable, which results in injected voltage with controllable magnitude and phase angle [10].

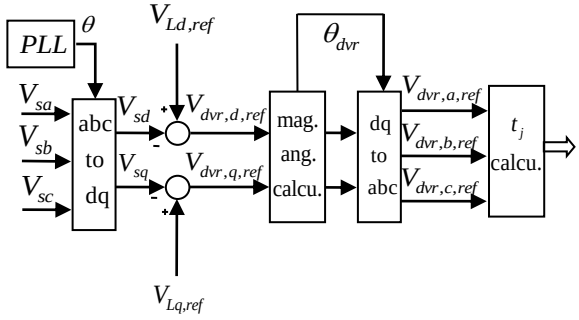


Fig. 6. Control block diagram of proposed DVR-FCL

4.3. Switching Time Intervals Calculation

According to the diagram presented in Fig. 6, the obtained reference voltages are used to calculate time interval of every transistor as described in [10]. Each

switching period is divided into six time intervals. Then, based on the states of the on and the off switches, output voltage of the inverter is obtained. This is demonstrated in Table 1.

Table. 1. On and off state of the inverter switches and the output voltage of inverter

Operation mode	On switches	Line-line output voltage		
		V_{ab}	V_{bc}	V_{ca}
I	S_1, S_4, S_5	V_{dc}	$-V_{dc}$	0
II	S_1, S_3, S_6	0	V_{dc}	$-V_{dc}$
III	S_2, S_3, S_5	$-V_{dc}$	0	V_{dc}
IV	S_2, S_4, S_5	0	$-V_{dc}$	V_{dc}
V	S_1, S_4, S_6	V_{dc}	0	$-V_{dc}$
VI	S_1, S_3, S_6	$-V_{dc}$	V_{dc}	0

5. Operation of Proposed Topology

An important concept to consider in explanation of the proposed DVR_FCL operation is the grid state with four operation modes, which are discussed below.

5.1. First Operating Mode: Normal State

In this operating mode, neither voltage fault nor current fault has occurred and so the grid is in the normal state. In this state S_1, S_2, S_3 and S_4 transistors and T_6 are turned off and in counterpoint, T_5 is turned on. In other words, FCL part of the proposed DVR-FCL is activated and because all diodes are in full conduction mode, no voltage drop appears across it [15]. At this time interval, application of the V_b in reverse polarity across D_b diode forces it to turn off. Hence, line current passes through D_1, D_2, D_3, D_4, DC reactor, DC voltage source and T_5.

5.2. Second Operating Mode: Current Fault Occurrence

When the short circuit fault occurs, the line current increases and consequently the RMS value of line current escalates [12, 15]. As it is explained in pervious section, control method detects current fault, hence S_1, S_2, S_3, S_4 and T_6 are turned off and T_5 is turned on. Because of inherent property of FCL in this operating mode, DC reactor, DC voltage source and pair of diodes (D_1 and D_4 or D_2 and D_3) become series with the grid and limit fault current enlargement [12]. Also D_b diode is reverse biased, so line current passes through pair of diodes, DC reactor and DC voltage source.

5.3. Third Operating Mode: Voltage Fault Occurrence

If a voltage fault like voltage sag happens, the control method detects fall in the magnitude of the load voltage. Consequently, T_5 is turned off and T_6 is turned on and DVR is enabled. Afterwards, inverter switches can be controlled in a procedure that is introduced before, so as to restore load voltage to nominal value. When T_5 is turned off, diode D_b is forced to turn on to circulate the DC reactor current until it drops to zero or voltage sag to be cleared (T_5 is turned on).

5.4. Fourth Operating Mode: Simultaneous Voltage and Current Fault Occurrence

It is obvious that DVR performs as series voltage source in the compensating mode [20]. Also it is evident that, additional voltage source intensifies short circuit current, which is undesirable. Conclusively, it is vital to disable DVR during current fault occurrence to prevent extension of fault current. Therefore, S_1, S_2, S_3, S_4 transistors and T_6 are turned off and T_5 is turned on. In this operating mode, diode D_b is reverse biased, too. Considering above-mentioned explanations, it is noticeable that in the simultaneous voltage and current fault, the FCL part of the proposed DVR-FCL operates.

6. Advantage of the Proposed Topology

Advantages of the proposed DVR-FCL can be classified into two categories: economical and technical. Both types are defined in the following. Also advantages of the proposed topology compared to the topology presented in [23] are explained.

6.1. Economic Advantages

The proposed DVR-FCL brings several economic profits in reduction of the used space and the cost of system functioning. These benefits include reduced number of utilized diodes, and injection transformers compared to case FCL and DVR are occupied simultaneously and separately. It is obvious that FCL and DVR with independent operations need two cooling systems which in this topology is reduced to one. Another feature of the proposed DVR-FCL is the elimination of bypass switches. When DVR is installed independently, bypass switches are considered to bypass secondary of injection transformers during DVR is disabled to lessen power loss and to prevent voltage waveform distortion. On the other hand, when the system is in the first, the second or fourth mode, DVR is disabled and FCL performs as bypass switches.

6.2. Technical Advantage

As expressed in the previous section, because of the reduced number of transformers, diodes and cooling system and deletion of bypass switches, power and command circuits include fewer elements which lead to a further simplified control method. Besides, maintenance and periodic checking in the DVR-FCL is simpler than the case in which FCL and DVR are used in separate form.

In [23] the FCL-DVR is presented which can be operated in similar conditions of the proposed DVR-FCL. But the proposed DVR-FCL has two major advantages compared to [23]. Firstly, in [23], when the gird is in the normal state, the DVR is activated and the reference voltage of the DVR is set to zero. Therefore, the switching loss in the normal state is high. Also, according to the mentioned defect, the life of the device declines gradually. Secondly, control and commutation circuit design of the crowbar bidirectional thyristors in [23] are more complicated than single switch, which is proposed in the DVR-FCL.

7. Simulations

To verify the performance of the proposed topology and control method, a three phase DVR-FCL prototype is simulated. The PSCAD/EMTDC software [25] has been used. For the safe operation of control switches in the absence of freewheeling paths, it is necessary to use a snubber circuit. Therefore, the proper snubber circuit design must be evaluated for T_{dvr} in proposed topology [26]. In the proposed DVR-FCL, a small R-C turn-off snubber connected across T_{dvr} is used to limit the device voltage to an appropriate level. It is important to note that the main focus of this paper was to introduce new topology and therefore the problem of optimized snubber design was not pursued further. The value of R and C in the snubber circuit are chosen as 10Ω and $0.002\mu\text{F}$, respectively. Fig. 7 depicts the used network and topology for simulation. In all simulations, it is assumed that the switches (transistors and IGBTs) are ideal while for the diodes $1V$ voltage drop is considered. Each S_i switch in this Figure is composed of transistor with anti paralleled diode. The load is an R-L load with 55mH inductance, 65Ω resistance for each phase. A balanced three phase source with $220\text{V}=1\text{pu}$ amplitude and 50Hz frequency is considered. According to Table 3, a small impedance is assumed for source, too, which is not shown in Fig. 7. The switching frequency of the inverter and its DC voltage are assumed 4kHz and 400V, respectively. The turn ratio of the transformers is chosen to be $1:1$. The used filter in the output of the inverter is a passive LC filter with damping resistor. The values for filter components are obtained by try and error method which are $L_f=2\text{mH}$, $C_f=35\mu\text{F}$,and $R_f=0.5\Omega$. The DC reactor, its resistance and series DC voltage source values are assumed to be $L_{dc}=20\text{mH}$, $R_{dc}=0.05\Omega$ and $V_b=4\text{V}$, respectively. The reference current of the DC reactor is assumed to be 5 times larger than the normal line current (when the line current reaches to that, the current fault condition is detected.). Also, complete explanation of the DVR-FCL and the grid characteristics are given in Tables 2 and 3, respectively.

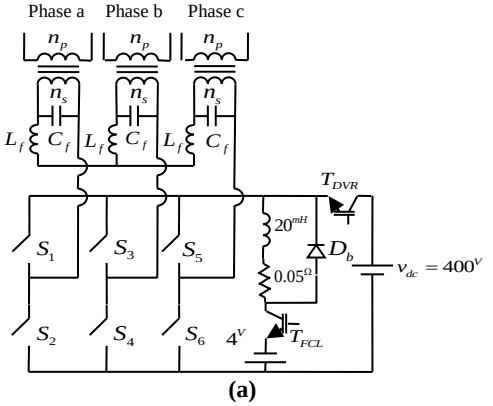
Four operating modes which are presented before are considered in one simulation. At the start of simulation until 0.04s, the grid is in the normal state. At this time, $0.3pu.$ voltage sag and $30°$ phase jump has occurred for 0.08s. In other words, magnitude of source voltage decreases to $154V$. Then at 0.12s, simultaneous voltage sag and three phase short circuit fault occur for time interval of 0.02s. Subsequently, for 0.01s, just three-phase short circuit fault has happened. At last from 0.15s to 0.2s, the state becomes normal again. {R3-6} It is worth considering that, if the current fault is not cleared in the specified duration of time, it is not the duty of proposed DVR-FCL to clear the fault, and it must be solve by other devices such as fault relay. Fig. 8 shows source voltage, load voltage and voltage across injection transformer.

Table. 2. DVR-FCL component characteristic

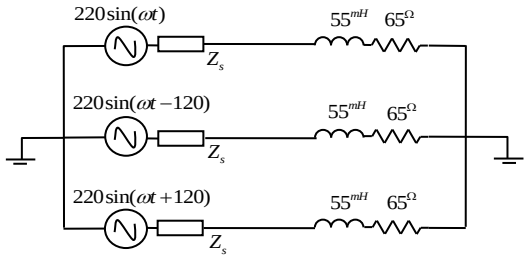
Parameter	Value	Parameter	Value
n_s/n_p	1/1	$V_{switch,on}$	1 V
L_f	2 mH	$V_{diode,on}$	1 V
C_f	35 μF	L_d	20 mH
R_f	0.5 Ω	R_d	0.05 Ω
v_{dc}	400 V	V_b	4 V

Table. 3. Grid component characteristic

Parameter	Value
Voltage source (max)	220 V
Frequency	50 Hz
Source impedance	0.6+j0.45 Ω
Load impedance	65+j17.28 Ω
Rated current	3.2 A



(a)



(b)

Fig. 7. (a) Used three phase DVR-FCL for simulation; (b) Used network for simulation

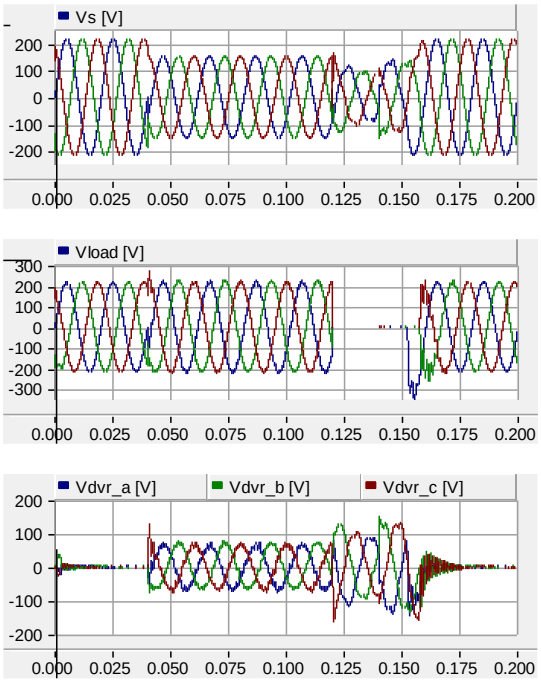


Fig. 8. Source voltage, load voltage and injection transformer's voltage

According to the presented Figure, it is evident that in the first operating mode T_{fcl} is turned on, hence FCL is enabled. As it is explained previously, FCL in the normal state behaves as a short circuit. At t=0.04s, voltage sag happens, then T_{dvr} is turned on and DVR is controlled in minimum voltage compensation method. Therefore, load voltage is restored to nominal value. This mode lasts for t=0.12s. At this instant, coincident voltage and current fault occur. Hence, T_{fcl} is turned on and T_{dvr} is turned off. In this operating mode, fault current is limited by DC reactor in FCL. This situation is continued until t=0.14s. At last, for period of 0.1s, only current fault happens and as pervious mode, FCL limits the fault current. Afterwards, at t=0.15s, the grid is cleared from any faults, so by turning T_{fcl} on, the DVR-FCL behave as short circuit. Fig. 9 shows source, DC reactor and D_b diode current, respectively.

In the normal condition, the DC reactor is charged through V_b with time constant of 0.4s. When the voltage sag is detected, T_{fcl} is turned. Therefore, the DC reactor current flows along D_b (in this case, because the voltage sag has occurred at 0.04s, the DC reactor current cannot reaches to steady state value.) until it falls to zero. Furthermore, because of the presence of the FCL at the instant of short circuit fault, rapid growth in fault current is limited properly.

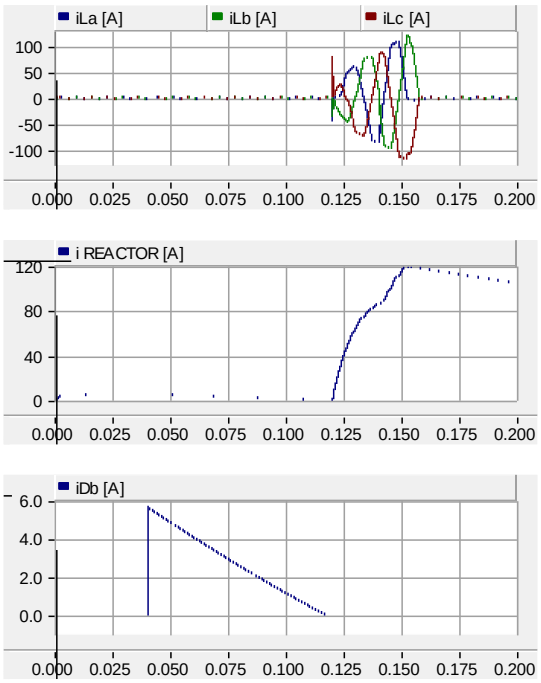


Fig. 9. Source current, DC reactor current and diode D_b current

{R3-6} As it was mentioned in the previous sections, choosing the value of L_d is one of the important parts of the design. A comparison of L_d value in the paper with that of [28] shows that, the FCL mostly affect the rate of current increment. In other words, if the higher value is chosen for L_d, the limitation effect of the FCL on the magnitude of the line current will be more distinctive.

In order to evaluate the performance of the proposed DVR-FCL in the sudden load changes, respective simulation has been done. The source impedance is assumed to be almost 5 times larger than the first simulation. Therefore, considerable voltage disturbance might be occurred by load change. Z_{L1}=65+j17.3Ω and Z_{L2}=25+j4.7Ω are considered as loads. Until 0.05s, Z_{L1} is connected to the grid and the maximum value of the line current is 3.1 A. In that moment, Z_{L2} is inserted to the grid, too. Therefore, the maximum value of the line current increases to 11.3 A. Then, 0.18

p.u. Voltage sag is appeared. According to the control method, the voltage sag is detected. Then, T_{fcl} and T_{dvr} are turned off and on, respectively. Afterwards, at 0.15s Z_{L2} is removed from the grid. Fig. 10 shows the source voltage, the loads voltage, and the line current, respectively.

It is evident in Fig. 10 that load current increment cause voltage drop across the source impedance. Therefore, voltage sag has occurred and the proposed DVR-FCL compensates the loads voltage to the nominal value.

{R3-4} In order to Fig. 7-a, the star point of injection transformer is not grounded. Therefore, it may be considered as problem during asymmetric faults. However, according to [9, 29], the proposed DVR-FCL can compensates asymmetric voltage disturbances and limits asymmetric short circuit faults.

In order to evaluate the performance of the DVR-FCL in asymmetric short circuit fault condition, the first simulation has been done again, when the two-phase short circuit fault is occurred. {R3-3} The presumed fault happens between the DVR-FCL and the load. Other assumptions and explanations are same as the first simulation. Fig. 11 shows {R3-3} the source voltage, the load voltage, the line current, and the DC reactor current, respectively.

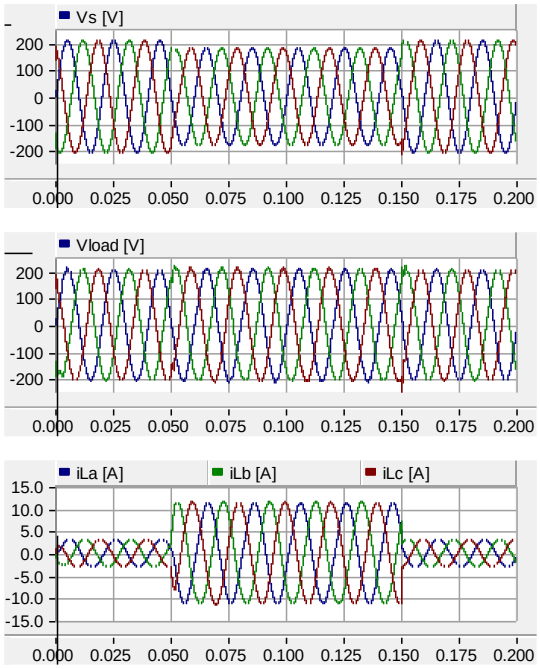


Fig. 10. Source voltage, loads voltage, and line current during load change.

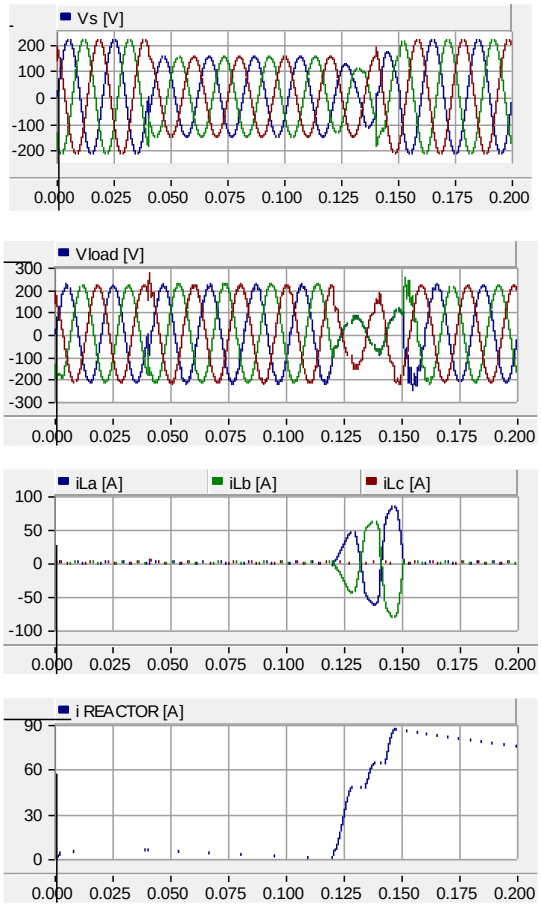


Fig. 11. Source voltage, load voltage, line current, and DC reactor current during asymmetric short circuit fault condition.

8. Conclusion

In this paper, a new topology is proposed. It is capable of controlling DVR and FCL in synchronous manner and also caused considerable cost save such as reduction in used diodes and transformer. According to the grid state, four operating modes can be considered which are 1) normal state, 2) current fault occurrence, 3) voltage fault occurrence, and 4) simultaneous voltage and current fault occurrence. A control method is proposed too which controls operation of the proposed DVR-FCL in every state. Also, simulation in the PSCAD/EMTDC software is completed which shows adaptable and proper performance of the proposed topology and control method.

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