New Coupled-Inductor Based Multilevel Inverter with Extension Capability

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Abstract :

Multilevel inverters have been developed due to limitations of the conventional two-level voltage source inverters (VSIs). Most of the topologies of multilevel inverters that have been presented in the literature are based on the sharing of the rated voltage between the switches so that the switches with lower voltage ratings can be used. In these topologies, the current rating of all of the switches is equal to the rated output current. Therefore, they may have limitations in high-current application. Recently, the coupled-inductor based multilevel inverter topologies have been presented to overcome the mentioned problem. In these topologies, the current rating of the switches is lower than the rated output current. In other words, these topologies can increase output current in comparison with the switches current. In this paper, a new generalized coupled-inductor based multilevel inverter is presented. The proposed topology consists of various coupled cells and can be extended to any number of voltage levels. This gives the generality and design flexibility for the proposed topology. If m cells are used in the proposed topology, the switches operate at the rated current equal to $1/2m$ of the rated output current. This shows a considerable in the switches current ratings. The number of voltage levels can be increased so that switches with lower current ratings can be used and at the same time, the quality of output voltage and current improves considerably. For the proposed topology, the pulse width modulation (PWM) method is also presented. The simulation results of the proposed 9-level inverter (in both single-phase and three-phase conditions) are presented to demonstrate the performance of the proposed topology.

Keywords: Multilevel inverter, coupled-inductor, high-current application.

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1. Introduction

The increased needs for power processing in the industrial fields have pushed the researchers to investigate for other solutions of power conversion beyond the conventional two-level inverters. The result of these investigations was introduction of a new family of power electronic inverters called multilevel inverters. The concept was first introduced by a three-level topology known as neutral point clamped (NPC) multilevel inverter [1]. This topology has been derived from the H-bridge inverter. Due to several key features of multilevel inverters, more researches have been conducted in this field and many other variants of multilevel inverters have been presented. The other two main topologies are the cascaded H-bridge (CHB) [2] and the flying-capacitor (FC) multilevel inverters [3]. However, from topological point of view, many other topologies of multilevel inverters have been derived from the main topologies [4-7]. Also, some topologies of multilevel inverters have been presented in order to reduce the components of them [8-18].

The most of the multilevel inverter topologies mentioned above use a power electronic arrangement so that the rated voltage of the inverter is shared between the switches and the switches with lower voltage can be used for high-voltage applications. However, in these topologies, the rated current of the switches is equal to the rated output current. As a result, they may not be well-suited for lower-voltage high-current applications. In these applications, it is necessary to provide various paths for current. This is addressed by paralleling the inverters using coupled-inductors or filter inductors.

Parallel-connected inverters [19-22], which either use current ripple cancellation or alternatively multilevel PWM output voltages, are widely used techniques for increasing the effective PWM and current ripple frequency above the device switching frequency. This often results in lower device losses, smaller inductors, a lowering of the current ripple magnitude, and a faster inverter transient response. Parallel-connected modules often use interleaved PWM and ac filter inductors connected between the modules to achieve high-frequency current ripple cancellation and a lower output current ripple [23]. Other coupled-inductor based topologies have been presented in [24-26]. In [23] single-phase two-switch and four-switch coupled-inductor inverter have been presented. The four-switch H-bridge coupled-inductor inverter produces a five-level output voltage which improves the output voltage quality. Pulse width modulation of the three-phase five-level split-wound coupled-inductor inverter has been presented in [24]. An active NPC (ANPC) based five-level coupled-inductor inverter and its three-phase variant has been presented in [25]. This topology consists of two stages, the high-current stage and the low-current stage. Each of these stages includes four power electronic switches in the single-phase scheme. In other words, half of the switches still operate with the rated output current while the high-current switches operate in fundamental frequency. However, extension of this topology to higher number of voltage levels has not been addressed. In [26] a single-phase coupled-inductor multilevel inverter has been presented. This inverter produces nine-level output voltage using fourteen-switch and two stacked-coupled inductors groups with 24 inductors. The proposed topology consists of several cells. For m cells the proposed topology, the current rating of the switches is $1/2m$ of the rated output current. Due to the cell-based architecture of the proposed topology, it can be extended to any number of voltage levels. Therefore, unlike the other coupled-inductor topologies, the proposed topology offers generality. In the next section, the proposed topology is introduced and analyzed. Following this section, the comparison of the proposed topology with other topologies is presented. After that the modulation method of the proposed topology is investigated. Finally, the simulation results of the proposed topology are presented in order to verify its operation and control.

2. Proposed Topology

Fig. 1 shows the proposed 9-level coupled-inductor inverter. As the figure shows, the 9-level inverter consists of two coupled cells. Each cell also consists of two coupled legs. The topology also includes one dc voltage source and the two switches S_a and S_b. These two switches operate in fundamental frequency and in complementary mode. In other words, one of them is turned on in the positive half cycle of the output voltage and the other is turned on in the negative half cycle of the output voltage. The two mentioned switches have been added to the topology in order to provide both negative and positive output voltage that is necessary for an inverter. If S_a is turned on, the average values of the voltages $v_{a1,n}$, $v_{b1,n}$, $v_{a2,n}$, and $v_{b2,n}$ are negative and therefore this switch is turned on during the negative half cycle of the output voltage. When the switch S_b is turned on, the average values of the mentioned voltage become positive indicating that the switch S_b is turned on during the positive half cycle. By proper switching of the proposed topology the 9-level output voltage can be obtained. Table I shows the switching table of the proposed 9-level inverter. As the table shows, all of the expected voltage levels can be obtained and therefore all of the sizes of all voltage steps are equal.

In order to avoid saturation in the coupled-inductors the average value of voltage on them should be zero and also their current should be balanced [25]. Also, the magnetic structure is considered to be ideal and no energy stored in the magnetic structure. Considering these conditions, the following equations can be written:

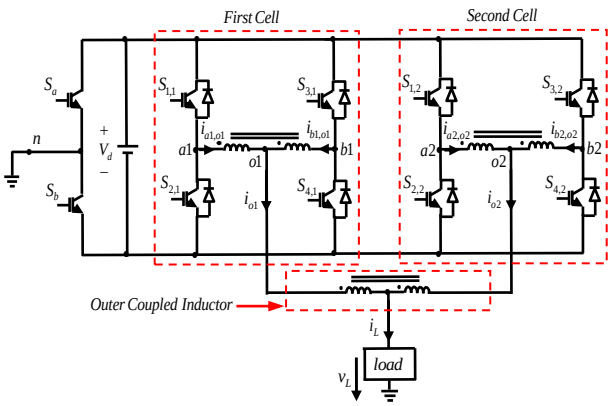


Fig.1. The proposed 9-level inverter using two cells

$$v_{a1,n} - v_{o1,n} = v_{o1,n} - v_{b1,n} \quad (1)$$

$$v_{a2,n} - v_{o2,n} = v_{o2,n} - v_{b2,n} \quad (2)$$

where, $v_{a1,n}$, $v_{b1,n}$, $v_{a2,n}$, $v_{b2,n}$, $v_{o1,n}$ and $v_{o2,n}$ are the voltages of the corresponding points in reference to the point n.

Using (1) and (2), the following equations can be obtained, respectively:

$$v_{o1,n} = \frac{v_{a1,n} + v_{b1,n}}{2} \quad (3)$$

$$v_{o2,n} = \frac{v_{a2,n} + v_{b2,n}}{2} \quad (4)$$

For the outer coupled-inductor, the voltage relation can be written as follows:

$$v_{o1,n} - v_L = v_L - v_{o2,n} \quad (5)$$

where, v_L is the load voltage.

Using (5), the load voltage is obtained as follows:

$$v_L = \frac{v_{o1,n} + v_{o2,n}}{2} \quad (6)$$

Applying Kirchhoff's current law (KCL) to the points $o1$ and $o2$ in Fig. 1, the following can be obtained:

$$i_{o1} = i_{a1,o1} + i_{b1,o1} \quad (7)$$

$$i_{o2} = i_{a2,o2} + i_{b2,o2} \quad (8)$$

where, i_{o1} and i_{o2} are the output current of the first and second cell, respectively. $i_{a1,o1}$ and $i_{b1,o1}$ are the current in the coupled-inductors of the first cell and $i_{a2,o2}$ and $i_{b2,o2}$ are the current in the coupled-inductors of the second cell.

Using (7) and (8) and considering equal current sharing between the coupled-inductors, the following relations can be obtained for currents:

$$i_{a1,o1} = i_{b1,o1} = \frac{i_{o1}}{2} \quad (9)$$

$$i_{a2,o2} = i_{b2,o2} = \frac{i_{o2}}{2} \quad (10)$$

For the outer coupled-inductor, the following relation can be written:

$$i_L = i_{o1} + i_{o2} \quad (11)$$

where, i_L is the load current.

The current through the coupled-inductors should be equal. Considering this fact and using (2), the following equation can be written:

$$i_{o1} = i_{o2} = \frac{i_L}{2} \quad (12)$$

Using (9)-(12), the following equation is obtained:

$$i_{a1,o1} = i_{b1,o1} = i_{a2,o2} = i_{b2,o2} = \frac{i_L}{4} \quad (13)$$

Equation (13) shows that the current through the switches $S_{i,j}$ ($i = 1,\cdots,4$, $j = 1,2$) is 0.25 of the load current. In other words, the load voltage is four times higher than the current through the switches. Therefore, the proposed topology can be used for high-current application using low-current rating switches.

Although the proposed topology with two cells has been investigated, the number of paralleled cells can be increased so that, for a constant output current, the current of switches can be reduced further and the number increases. However, it should be noted that the number of cells is in the form of 2^i. This is because of the fact that each two coupled-inductors gather the output current of two similar units. The proposed generalized coupled-inductor multilevel inverter is shown in Fig. 2. In general, if the proposed topology consists of m cells, the following equations can be written:

$$N_{switch} = 4m + 2 \quad (14)$$

$$N_{level} = 4m + 1 \quad (15)$$

$$N_{inductor} = 2m - 1 \quad (16)$$

where, N_{switch}, N_{level}, and $N_{inductor}$ are the number of switches, number of voltage levels and number of coupled-inductors, respectively.

Using (14) and (15), the following relation can be obtained:

$$N_{switch} = N_{level} + 1 \quad (17)$$

In general, the relation of load current and the current through the switches can be written as follows:

$$i_{aj,oj} = i_{bj,oj} = \frac{i_L}{2m} \qquad j = 1,2,\cdots,m \quad (18)$$

Equation (18) shows that the current through the switches decreases considerably as the number of cells increases.

TABLE.1. SWITCHING STATES OF PROPOSED 9-LEVEL INVERTER

Modes	Output voltage	Outer coupled inductors voltages		Coupled inductors voltages of each cell				Switches states									
	v_L	v_{o1}	v_{o2}	v_{a1x}	v_{b1x}	v_{a2x}	v_{b2x}	S_a	S_b	S_{11}	S_{21}	S_{31}	S_{41}	S_{12}	S_{22}	S_{32}	S_{42}
1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	0	1	1	0	1	0	1	0	1	0
2	$3V_{dc}/4$	$V_{dc}/2$	V_{dc}	0	V_{dc}	V_{dc}	V_{dc}	0	1	0	1	1	0	1	0	1	0
3		$V_{dc}/2$	V_{dc}	V_{dc}	0	V_{dc}	V_{dc}	0	1	1	0	0	1	1	0	1	0
4		V_{dc}	$V_{dc}/2$	V_{dc}	V_{dc}	0	V_{dc}	0	1	1	0	1	0	0	1	1	0
5		V_{dc}	$V_{dc}/2$	V_{dc}	V_{dc}	V_{dc}	0	0	1	1	0	1	0	1	0	0	1
6	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	V_{dc}	0	V_{dc}	0	0	1	1	0	0	1	1	0	0	1
7		$V_{dc}/2$	$V_{dc}/2$	0	V_{dc}	0	V_{dc}	0	1	0	1	1	0	0	1	1	0
8		$V_{dc}/2$	$V_{dc}/2$	V_{dc}	0	0	V_{dc}	0	1	1	0	0	1	0	1	1	0
9		$V_{dc}/2$	$V_{dc}/2$	0	V_{dc}	V_{dc}	0	0	1	0	1	1	0	1	0	0	1
10		0	V_{dc}	0	0	V_{dc}	V_{dc}	0	1	0	1	0	1	1	0	1	0
11		V_{dc}	0	V_{dc}	V_{dc}	0	0	0	1	1	0	1	0	0	1	0	1
12	$V_{dc}/4$	$V_{dc}/2$	0	V_{dc}	0	0	0	0	1	0	1	1	0	0	1	0	1
13		$V_{dc}/2$	0	0	V_{dc}	0	0	0	1	0	1	1	0	0	1	0	1
14		0	$V_{dc}/2$	0	0	V_{dc}	0	0	1	0	1	0	1	1	0	0	1
15		0	$V_{dc}/2$	0	0	0	V_{dc}	0	1	0	1	0	1	0	1	1	0
16	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1
17		0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0
18	$-V_{dc}/4$	$-V_{dc}/2$	0	$-V_{dc}$	0	0	0	1	0	0	1	1	0	1	0	1	0
19		$-V_{dc}/2$	0	0	$-V_{dc}$	0	0	1	0	1	0	0	1	1	0	1	0
20		0	$-V_{dc}/2$	0	0	$-V_{dc}$	0	1	0	1	0	1	0	0	1	1	0
21		0	$-V_{dc}/2$	0	0	0	$-V_{dc}$	1	0	1	0	1	0	1	0	0	1
22	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}$	0	$-V_{dc}$	0	1	0	0	1	1	0	0	1	1	0
23		$-V_{dc}/2$	$-V_{dc}/2$	0	$-V_{dc}$	0	$-V_{dc}$	1	0	1	0	0	1	1	0	0	1
24		$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}$	0	0	$-V_{dc}$	1	0	0	1	1	0	1	0	0	1
25		$-V_{dc}/2$	$-V_{dc}/2$	0	$-V_{dc}$	$-V_{dc}$	0	1	0	1	0	0	1	0	1	1	0
26		0	$-V_{dc}$	0	0	$-V_{dc}$	$-V_{dc}$	1	0	1	0	1	0	0	1	0	1
27		$-V_{dc}$	0	$-V_{dc}$	$-V_{dc}$	0	0	1	0	0	1	0	1	1	0	1	0
28	$-3V_{dc}/4$	$-V_{dc}/2$	$-V_{dc}$	0	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	1	0	1	0	0	1	0	1	0	1
29		$-V_{dc}/2$	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$	$-V_{dc}$	1	0	0	1	1	0	0	1	0	1
30		$-V_{dc}$	$-V_{dc}/2$	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$	1	0	0	1	0	1	1	0	0	1
31		$-V_{dc}$	$-V_{dc}/2$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	1	0	0	1	0	1	0	1	1	0
32	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	1	0	0	1	0	1	0	1	0	1

The proposed topology can be easily extended to any number of phases. As an example, the three-phase 9-level inverter based on the proposed topology is shown in Fig. 3. The three-phase system includes three similar structures and their operation principle is the same. Clearly, the reference voltage of the phases has a phase angle difference equal to 120°.

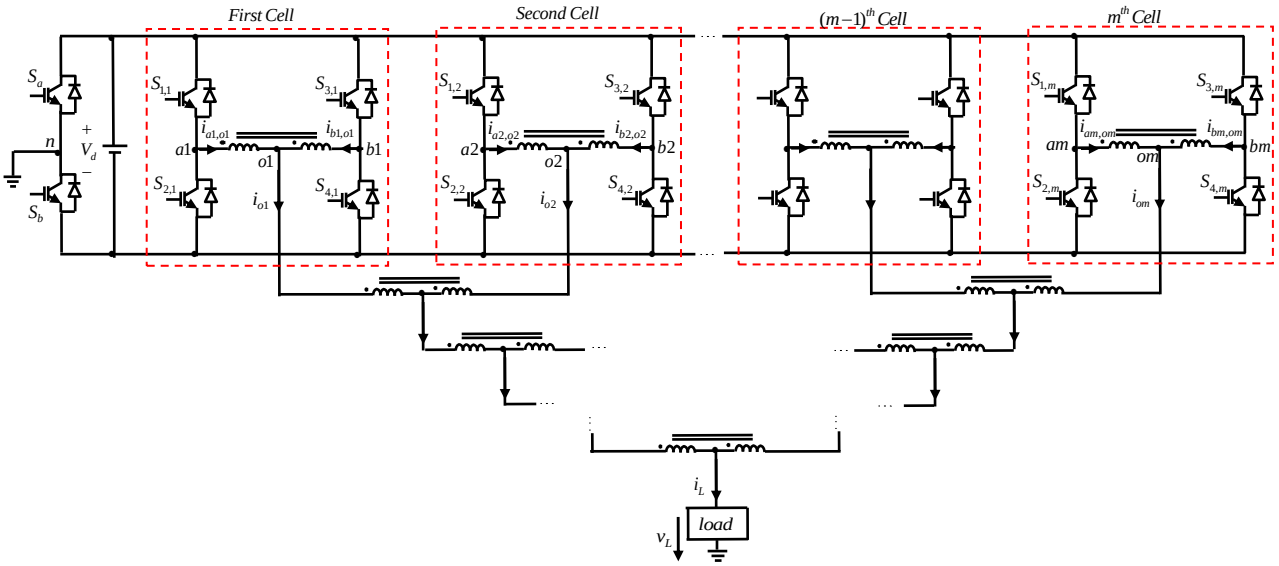


Fig. 2. Generalization of proposed coupled-inductor multilevel inverter

3. Comparison of Proposed Inverter with Other Inverters

In this section the comparison of the proposed topology with other topologies is presented in order to verify its potential advantages and disadvantages. For fair comparison, the proposed topology is compared with two types of multilevel inverters: the conventional types and the coupled-inductor based multilevel inverters. In the first comparison the proposed topology is compared with conventional 9-level inverters. Since the topologies presented for coupled-inductor based multilevel inverters are limited, so the comparison with the ones only with the same number of voltage levels is mainly not possible. So the second comparison is made with two coupled-inductor based inverters with 9 and 5 output voltage levels Therefore, in order to have a fair comparing, the number of components is normalized by dividing them to the number of voltage levels. Generally the comparison is drawn in terms of the number of components and the switches and inverter total current ratings

In the first comparison, the proposed topology is compared with the conventional 9-level inverters. The proposed 9-level inverter uses 10 switches while for the same number of voltage levels, the CHB, NPC and FC multilevel inverters use 16 switches. So in comparison with three mentioned conventional topologies, the proposed structure with lower number of switches, has a lower switching losses and also lower conduction losses. Furthermore, the proposed topology needs three coupled inductors while the NPC multilevel inverter uses 4 flying capacitor and 6 extra clamping diodes and the FC topology uses 7 flying capacitors. On the other hand, the proposed topology does not have any flying capacitors and extra clamping diodes. As a result, in the proposed structure, there are not the complicated controls of capacitors voltage balance and output voltage fluctuation due to the capacitors. Also, totally the number of components in proposed structure is lower than the mentioned conventional topologies then the losses of proposed structure are lower than them. From the view point of the switches ratings, in the proposed topology the switches current rating is 0.25 of the output current while in the conventional topologies the current rating of all of the switches is equal to the nominal output current. As a result, the proposed topology is suitable for high-current applications while the conventional topologies are suitable for high-voltage applications.

In the second comparison, the proposed topology is compared with the coupled-inductor based multilevel inverters. Table II shows the comparison results of the proposed 9-level inverter with 5-level and 9-level coupled-inductor based inverters presented in [25] and [26], respectively. The [25] presents a 5-level inverter using a coupled inductor, one dc source, 8 bidirectional power switches, and also split of dc-link capacitors. Also, in [26] a coupled inductor based multilevel inverter is presented. This topology for generating 9-level output voltage uses two stacked-coupled inductors groups including 24 inductors (each stacked-coupled inductors group include 12 pair wise coupled inductors), one dc source, 10 bidirectional power switches, 4 three-pole power switches (each three-pole power switch has one transistor and two diodes with midpoint), and also split of dc link capacitors. As shown in table (II), the proposed topology to generate the 9-level voltage requires one dc source with no need for dc-link capacitors. Then, the complicated control strategy of the capacitors and their voltage balancing is avoided in the proposed structure in comparison with

TABLE 2. COMPARISON RESULTS OF THE PROPOSED INVERTER WITH COUPLE-INDUCTOR BASED INVERTERS

Topology	Levels No.	Switch/level	Inductor/level	dc capacitor/level	Switches current rating**
Proposed	9	1.11	0.66	0	$2\times1pu+8\times0.25pu$
[18]	5	1.6	0.4	0.4	$4\times1pu+4\times0.5pu$
[19]	9	1.55*	2.66	0.22	$2\times1pu+12\times0.25pu$

*Generally the switch component in the switch/level ratios indicates the number of bidirectional power switches while in [18] it is combination of 10 bidirectional power switches+ 4 three-pole power switches that each three-pole power switch has one transistor and two anti-parallel diodes with midpoint

**The switches current rating in pu considering the peak output current as the base value

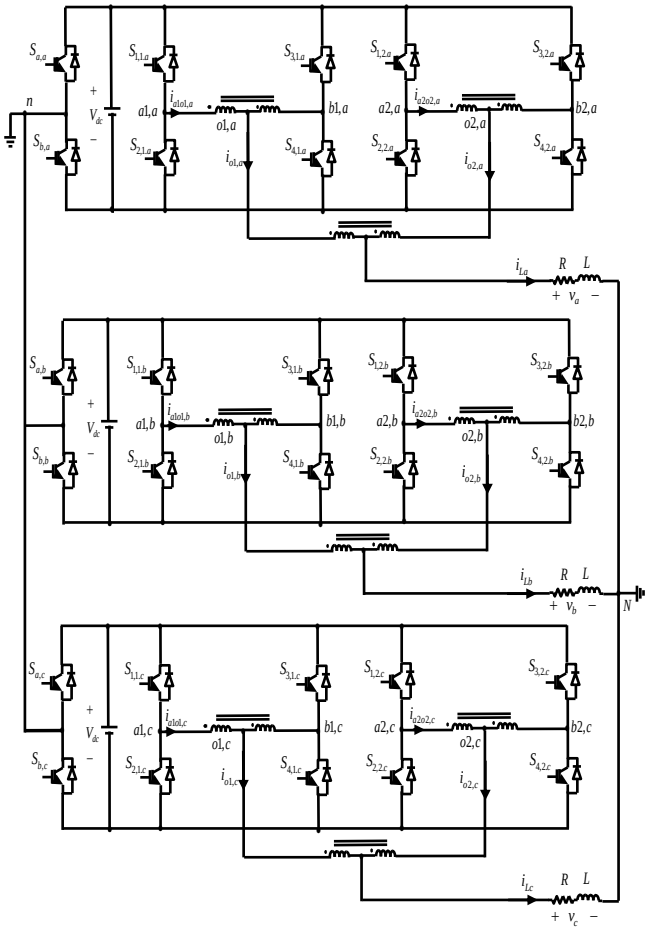


Fig.3. Three-phase 9-level inverter based on the proposed topology

topologies presented in the table. The proposed topology uses less number of switch/level ratios in comparison with topologies in the table. This topology uses three coupled inductors that cause to 80% percent of the switches have the current rating equal to 0.25 of the output current rating while in [26], by using two stacked-coupled inductors groups that includes 24 inductors, the same result is achieved meaning that the current rating of the low current switches is equal to 0.25 of the output current rating and two other switches operate with full output current. By considering the number and structure of coupled inductors used in the proposed 9-level and presented 9-level inverter in [26], it can be found that using three coupled inductors (totally with six inductors) is more suitable and applicable than the two stacked-coupled inductors groups with 24 inductors (each stacked-coupled inductors group include 12 pair wise coupled inductors) which have more cupper losses and also need more bulky core because of the more number of inductors. Moreover in [25] the ratio (number of low current switches/total number of switches), is 50% and the current rating of low current switches is equal to half of the output current rating and the other switches have the current equal to the full output current. So the reduction of number of switches and switches current stress are the main advantages of utilizing the new inverter in comparison with relevant ones. As a result, the proposed topology is suitable for high-current applications more than the other relevant coupled inductor and conventional multilevel inverters.

4. Modulation Method of Proposed Topology

Fig. 4 shows the modulation method of the proposed topology in general. As the figure shows, the reference waveform ($v_{L,ref}$) is modified and then used for modulation. In the positive half cycle, $v_{L,ref}$ is used and in the negative half cycle $1-|v_{L,ref}|$ is used for modulation. This can be implemented by a comparator and a selector. The gate signals of the switches S_a and S_b are generated by comparing the reference waveform with the zero level. For the other switches, the gate signals are produced by comparing the modified reference waveform with suitable carrier waveforms which are high-frequency triangular waveforms. The typical $(2j-1)th$ carrier waveform has an initial phase angle equal to $\frac{(j-1)\pi}{m}$ and the typical carrier $(2j)th$ has an initial phase angle equal to $\frac{(m+j-1)\pi}{m}$. Therefore, two carrier waveforms that belong to an H-bridge, have a phase angle difference equal to π. Also, the phase angle difference between a

carrier waveform of an H-bridge and its corresponding carrier waveform of the adjacent H-bridge is equal to $\frac{\pi}{m}$. The typical switch $S_{1,j}$ operates in complementary with the switch $S_{2,j}$ and $S_{3,j}$ operates in complementary with the switch $S_{4,j}$. From Fig. 4 it is clear that the switch $S_{1,j}$ switch $S_{3,j}$ is turned on when $v_{ref} > Carrier\,(2j)th$. is turned on when $v_{ref} > Carrier\,(2j-1)th$ and the

For the proposed 9-level inverter, 4 carrier waveforms are used. The initial phase angle of the first carrier waveform is 0 and that of the second carrier waveform is 180°. These two carriers belong to the first cell. The third and fourth carrier waveforms that belong the second cell have an initial phase angle of 90° and 270°, respectively.

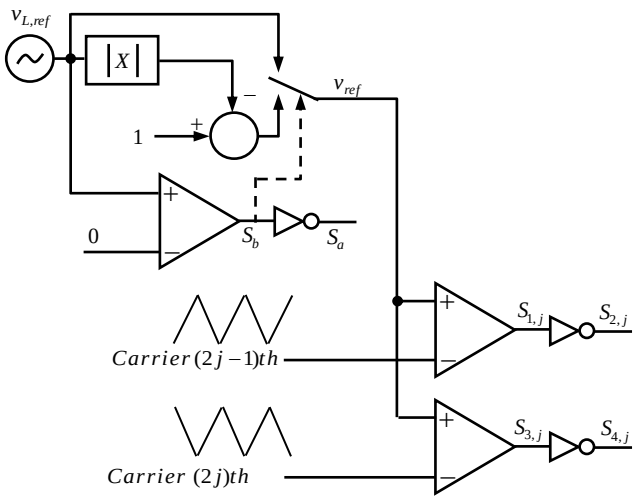


Fig.4. Modulation method of the proposed multilevel inverter

For the proposed Three-phase topology the same modulation method as shown in Fig. 4, is used. In other words, three similar modulation scheme (Fig. 4) are used where the only difference for different phases is the reference voltage ($v_{L,ref}$). The reference voltages for the three-phase topology have 180° phase shift.

5. Simulation Results

In this section, the simulation results of the proposed topology have been presented its operation and control. The simulations have been carried out in the PSCAD/EMTDC software. For simulations, the9-level inverter is considered and it is designed to produce 110V RMS output voltage. Therefore, the value of the dc voltage source is about $110\sqrt{2} = 155.6V$. The load is considered to be inductive with the resistance and inductance of 25Ω and 15mH, respectively. The switching frequency and the load voltage fundamental frequency are 8kHz and 50Hz, respectively. The self and mutual inductance of the coupled-inductors are 1mH and 0.9mH, respectively.

Fig. 5 shows the simulation results of the proposed single-phase 9-level inverter. Fig. 5(a) shows the voltage waveforms. The top trace in Fig. 5(a) shows the output voltage of the first cell, the middle trace shows the output voltage of the second cell and the bottom trace shows the load voltage. As the figure indicates, the number of levels of the output voltage of the cells is five. However, their phase shift is in a way that the load voltage is a 9-level voltage. Fig. 5(b) shows the current waveforms. In the top trace of this figure, the current through the coupled-inductor of the first cell and also the output current of the first cell can be seen. The middle trace of the figure indicates the current through the coupled-inductor and the output current of the second cell. The bottom trace shows the load current. As the figure shows, the output current of the cell is double of the current through the coupled-inductor and also its ripple is much lower. Also, the load current is double of the output current of the cells and its ripple is lower. Therefore, the load current is four times higher than the coupled-inductor current and its ripple is extremely lower. Considering that the current through the coupled-inductors is equal to the switches current, the switches operate in rated current of 0.25 of the load current. This makes the proposed topology suitable for high-current applications.

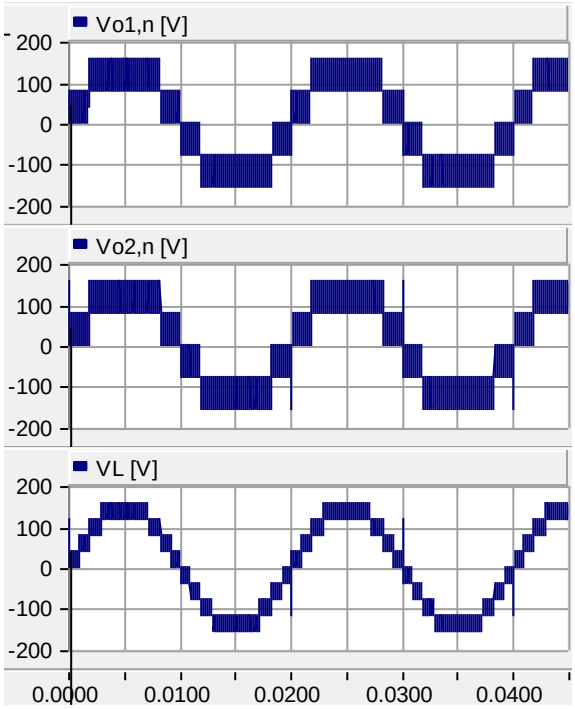
The switching pulses of the inverter are shown in Fig. 6. To be brief, the switching pulse of one of each pair of complementary switches is shown. As the figure shows, the switch S_a operates at fundamental frequency while other switches operate at high-frequency.

In Fig. 7 the zoomed-in view of voltage across the coupled inductors are shown. The voltages are pulsed voltages with the mean value of zero.

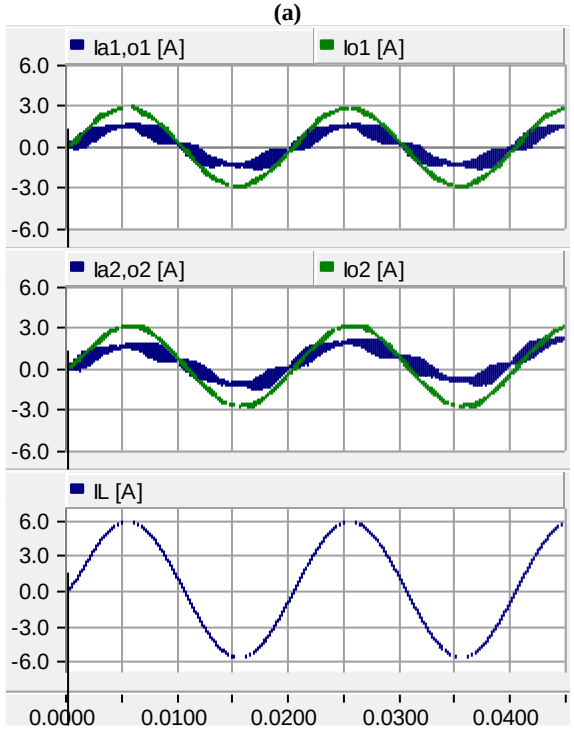
In no-load condition, the current through the coupled inductors are shown in Fig. 8.

Fig. 9 shows the simulation results of the proposed three-phase 9-level inverter. As the three-phase scheme consists of three single-phase units and the neutral point of the load is grounded, the results of the three-phase inverter are similar to that of the single-phase inverter with proper phase angle differences between the phases.

Fig. 9(a) shows the three-phase voltage waveforms. The top trace in Fig. 9(a) shows the output voltages of the cells, the middle trace shows the three-phase load voltages and the bottom trace shows the line voltage. The output voltages of the cells are 5-level voltages while the load voltage is a 9-level voltage.



(a)



(b)

Fig.5. Simulation results of the proposed single-phase 9-level inverter, (a) top to bottom: output voltage of the first cell, output voltage of the second cell, load voltage, (b) top to bottom: current through the coupled-inductor of the first cell and the output current of the first cell, current through the coupled-inductor of the second cell and the output current of the second cell, load current

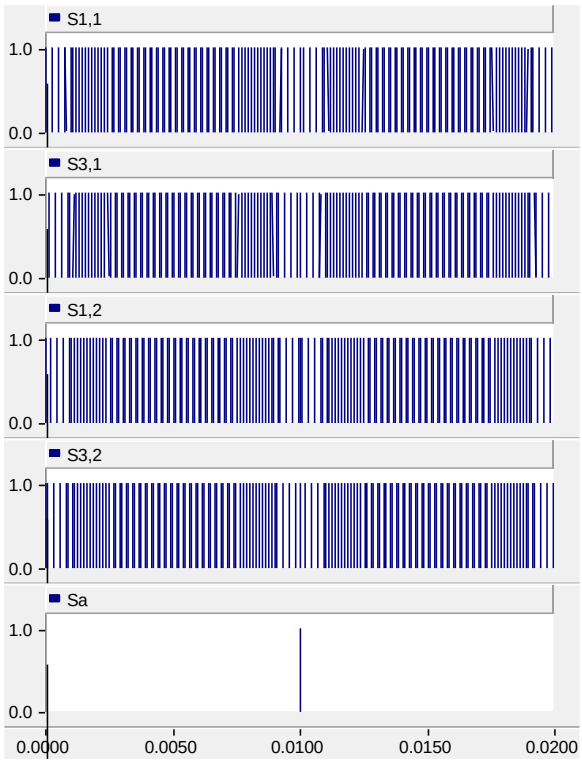


Fig.6. The switching pulses of the proposed inverter

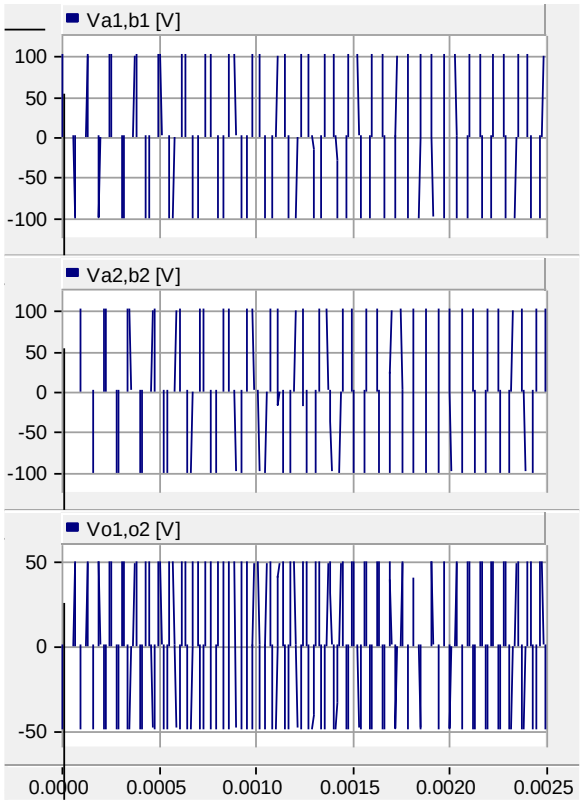


Fig.7. Zoomed-in view of voltage across the coupled inductors

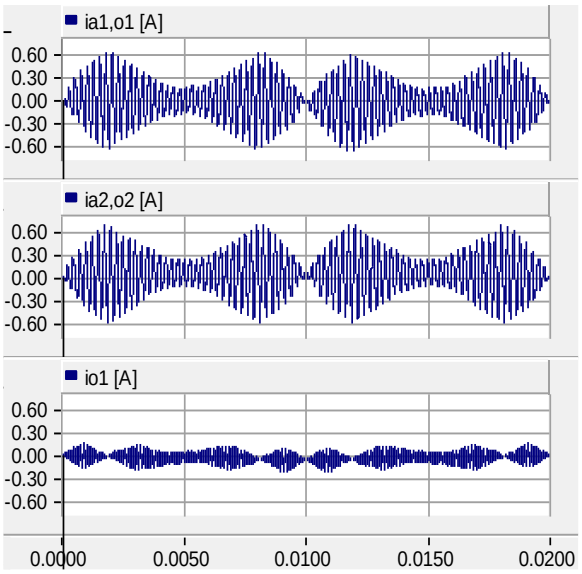
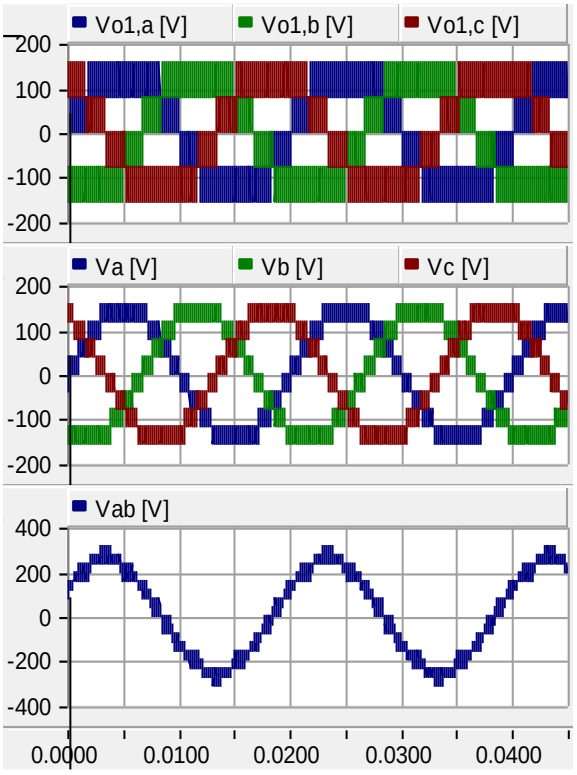


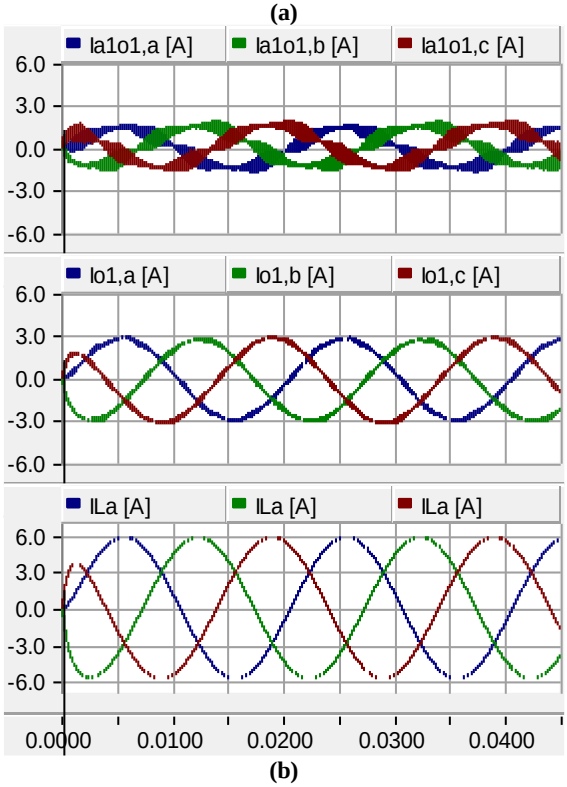
Fig. 8. No-load current through the coupled inductors

Fig. 9(b) shows the current waveforms. In the top trace of this figure, the current through the coupled-inductor of the cells are presented. The middle trace of the figure shows the output current of the cells. The bottom trace shows the three-phase load currents. As the figure shows, the output currents of the cells are double of the currents through the coupled-inductors and also their ripples are much lower. Also, the load currents are double of the output currents of the cells and their ripples are lower. Therefore, like the single-phase scheme, the load current is four times higher than the coupled-inductor current and its ripple is considerably lower.

In Fig. 10, harmonic spectrum of the current through the coupled-inductor of the first cell (Fig. 10(a)) and the output current of the first cell (Fig. 10(b)) are shown. As the figures show the harmonic content of the current through the coupled inductor (harmonics of $i_{a1,o1}$) is higher than that of the output current of the first cell (harmonics of i_{o1}). Also, harmonics of i_{o1} appear in frequencies that are twice of the frequencies in which the harmonics of appear. This is because of using interleaved modulation. The harmonic spectrum of the output current is not shown since they are negligible in comparison with the harmonics of the mentioned currents.



(a)



(b)

Fig.9. Simulation results of the proposed three-phase 9-level inverter, (a) top to bottom: output voltages of the first cells, output voltages of the second cells, load voltages, (b) top to bottom: currents through the coupled-inductor of the first cells and the output currents of the first cells, currents through the coupled-inductor of the second cells and the output currents of the second cells, load currents

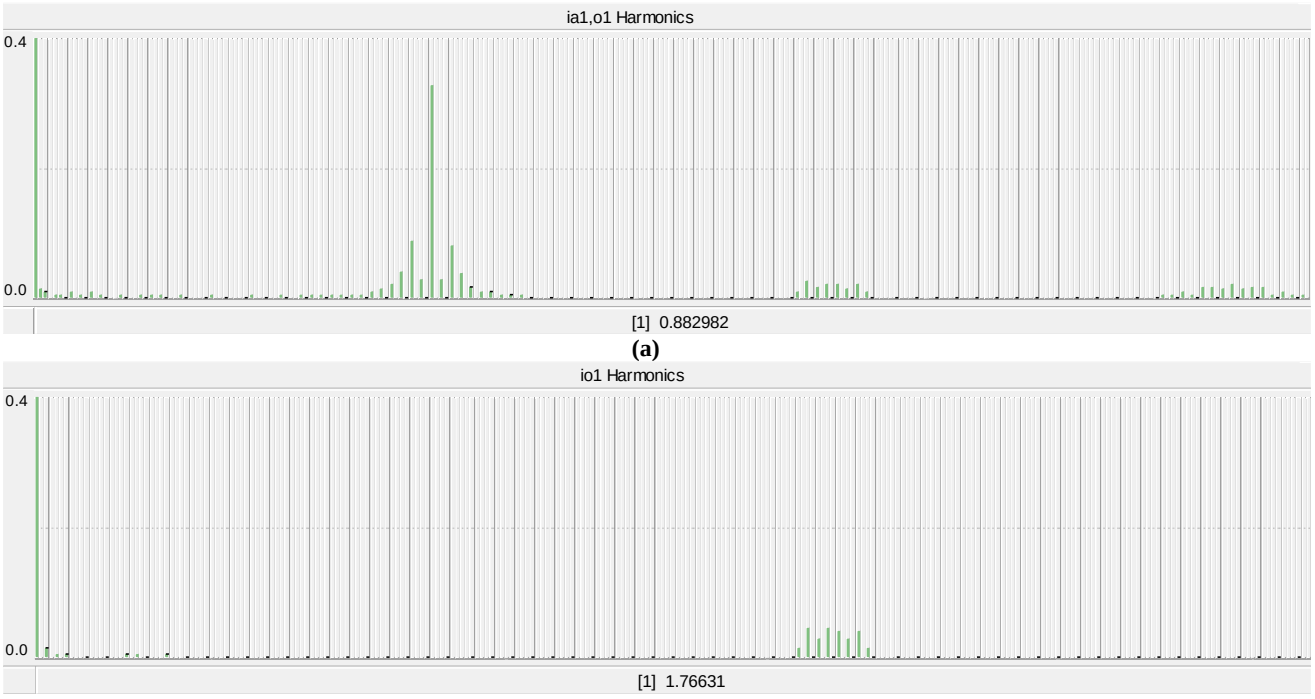


Fig.10. Harmonic spectrum for (a) current through the coupled-inductor of the first cell, (b) the output current of the first cell

6. Conclusion

New topology of coupled-inductors based multilevel inverter has been presented in this paper. The proposed topology uses several coupled cells. From the structure point of view, the proposed topology owns the capability of extending to any number of voltage levels. This results in generality of the proposed topology. As it has been investigated, the current through the switches depends on the number of cells. Higher number of cells results in more reduction of the switches' current. On the other hand, the quality of the output voltage and current improves. As an example, for the proposed 9-level topology, the current through the switches is 0.25 of the output current. The proposed topology has been demonstrated by simulation results. For the simulations in both single-phase and three-phase conditions, the 9-level topology has been used. As the results showed, the expected voltage levels have been produced successfully and output current increase (or switch current decrease) is achieved.

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