

# Comprehensive Evaluation of Crosstalk and Delay Profiles in VLSI Interconnect Structures with Partially Coupled Lines

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## Abstract :

In this paper, we present a methodology to explore and evaluate the crosstalk noise and the profile of its variations, and the delay of interconnects through investigation of two groups of interconnect structures in nano scale VLSI circuits. The interconnect structures in the first group are considered to be partially coupled identical lines. In this case, by choosing proper values for different parameters, the crosstalk noise, when the victim line stays ahead of the aggressor line can be reduced up to 92% in comparison to when it is behind the aggressor line. The second group consists of a victim line shorter than the aggressor line. In this case, if the parameters are properly optimized, when the victim line is placed at the end of the aggressor line, the crosstalk noise can be reduced up to 86% in comparison to the case when the victim line is placed at the beginning.

**Keywords:** Interconnect, Crosstalk, partially coupled lines.

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## 1. Introduction

along with transistors, the interconnects shrink in size as well. But interconnects do not scale as much as the transistors do, and as a result their time delay is becoming dominant comparing to the gates' time delay. On the other hand, regarding to the decrease in interconnects spacing and increase of their aspect ratio, the crosstalk noise will no longer be negligible, which cause the performance and the reliability of the circuits to decline [1-4].

In recent years a number of researchers have coped with the interconnect problems such as crosstalk and delay for different technologies [4, 5, 6] using ITRS predictions [7]. Among the problems mentioned above, crosstalk plays a key role in signal integrity and performance of systems [8]. Thus, a comprehensive analysis of this parameter is necessary and needed to be reduced as much as possible.

Due to the importance of crosstalk noise, various methods for its analysis and reduction have been investigated, such as: shielding methods [9-11], the repeater insertion [12-16], the device sizing [17-19], various routing techniques [20-27] and input coding [28-33].

In parallel interconnect structures, the coupled capacitance is the main source of the crosstalk noise, and as it gets larger, more crosstalk voltage increases. In most crosstalk reduction methods and vast researches, the interconnect lines have been considered to be parallel with fully length coupling. In this work, different groups of structures with partially coupled or different lengths are evaluated and the crosstalk voltage and the delay are studied. Some of structures have been studied briefly in [34]. In this paper, different features, various positions, and buffer direction related issues have been studied more precisely, in details, and with more accuracy.

Interconnects and wires are used in integrated circuits, bonding wires, frame leads, wiring connections between various ICs mounted on a PCB and so on. Hence, investigation into the wires parameters are essential and can be conducted in different manners such as: studying the role of parameters of one wire, statistical studies of a group of wires, technology issues, wires induced faults in ICs, systems, and PCBs and etc. It's not possible to investigate all aspects of interconnects and wires in different applications in one research work. As such, this research focuses on several important issues such as the effects of changing the position, overlap lengths, overall length, and the buffer directions.

Most of the crosstalk models are based on the capacitive coupling. Hence, structures in this work are modeled using a lumped RC network, in order to extract simplified analytical expressions. We clearly notice that the inductive effects should be considered in modeling interconnects at very high frequencies, lower fall and rise times for fast switching signals, and high

As technology merges into deep submicron and nanometer regions,

conductive interconnect systems. However, in this research, in order to mainly focus on the principle goal of crosstalk modeling in partially coupled structures, the inductive effects are not taken into account. Although the inductance effects of wires could be issue in very long and very low resistive wires at the frequencies over several 10 GHz, almost all of interconnects in today VLSI circuits can be modeled by several L-section or distributed RC circuit model. As a result, considering this assumption the wires model will not be dependent to the frequency operation of the circuit. The drivers are modeled by a resistance and a capacitance as well. The simulation analyses of such structures are conducted using the simulation tool HSPICE. We consider several assumptions in this paper such as: 1) the input signal of the aggressor line is assumed to be a step waveform. Indeed the input step waveform becomes realistic and close to real situations using a buffer so that the output signal of the buffer will be a real signal applied to the wire; 2) the input of the victim line is constant with the value of  $V_{DD}$  so that the output of the victim driver would be connected to a ground.

The rest of this article is organized as follows. First, the assumptions and basic information related to two general case study structures are presented in Section II. A few comments, necessary for understanding the structures, are listed in this section. Next, a group of structures consisting of two similar partially coupled interconnects (named as SAME LENGTH or "SL") are introduced in Section III. Then, in Section IV the crosstalk in a group of structures consisting of two interconnects with different lengths (named as LONG AGGRESSOR SHORT VICTIM or "LA\_SHV") are evaluated. Finally, concluding remarks are provided in Section V.

## 2. Fundamental Concepts for Evaluating the Crosstalk Noise

Two structures shall be investigated in this work. In both structures  $(W/L)_a$ ,  $(W/L)_v$ ,  $I_{n_a}$ ,  $I_{n_v}$  and  $C_L$  denote the aggressor driver size, the victim driver size, the aggressor input, the victim input, and the load capacitance, respectively. The values of these parameters are listed in table 1. For evaluating the structures, the aggressor signal is assumed to be almost an ideal step waveform, so its rise time is set to 20ps. The interconnects dimensions are extracted from PTM library [35] in 90nm technology.

To have an intuitive understanding of the structures' evaluation, it is necessary to mention several points:

i) If the rise time of the signal decreases, the signal will contain higher frequency components so that the coupling capacitance impedance ( $1/sC_c$ ) gets smaller.

This will cause the voltage signal to pass easier and the crosstalk noise voltage to increase.

ii) In both case studies that will be analyzed in the following sections, the victim line in B structures is placed slightly ahead of the aggressor line driver. Hence, the aggressor signal in these structures should pass a distance in order to reach the coupling region. Consequently, the sharpness of the signal weakens and causes the crosstalk amplitude to decline. This leads B structures in both case studies to have always smaller crosstalk noise rather than A structures.

**Table. 1. The values of circuit parameters**

Parameters	Value
Technology	90 nm
Interconnect width	0.2 $\mu\text{m}$
Substrate height	0.3 $\mu\text{m}$
Interconnect thickness	0.5 $\mu\text{m}$
Interconnect space	0.4 $\mu\text{m}$
$\epsilon_r$	2.8
$\rho$	$2.8 \times 10^{-8} \Omega \cdot \text{m}$
$T_r$	20 ps
$V_{DD}$	1 V
$C_L$	5 fF
$R_d$ (for min size driver)	9.69 K $\Omega$
$C_p$ (for min size driver)	0.658 fF
$R_n$ (for min size transistor)	1.68 K $\Omega$
Line length SL	1 mm
Coupled length SL	0.2 mm
$(W/L)_a$ SL	30
$(W/L)_v$ SL	10
Aggressor length LA_SHV	1 mm
Victim length LA_SHV	0.2 mm
$(W/L)_a$ LA_SHV	30
$(W/L)_v$ LA_SHV	10

iii) All structures are implemented using lumped RC model. The reason is that the purpose of this article is to compare two different structures in each case study for the crosstalk noise. Therefore, a simple model would be sufficient. Although the RC model is not accurate as RLC model, the acceptable accuracy can be confirmed by HSPICE results.

iv) Since the inputs of victim lines don't switch and are always connected to  $V_{DD}$ , only the NMOS transistor in an inverter (buffer) remains on. This transistor can be modeled with a resistance  $R_n$  with the following expression.

$$R_n = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{DD} - V_{th})} \quad (1)$$

The value of this resistance is shown in table 1.

v) The coupled length in LA\_SHV case study is the same as the victim length. In this article, the victim length for this group of structures is referred to as the coupled length.

Interconnects are assumed to be inhomogeneous microstrips, placed on a substrate with a relative permittivity of  $\epsilon_r$ , while the top layer is assumed be air with the relative permittivity of 1. The equations used for calculating the per-unit-length (PUL) wire resistance and wire capacitance for microstrip structures are as follow [36]:

$$R = \rho \frac{1}{A} = \rho \frac{1}{W \cdot Th} \Omega/m \quad (2)$$

$$C_w = \frac{2\pi\epsilon_0\epsilon_{eff}}{\ln\left[\frac{8H}{W} + \frac{W}{4H}\right]} F/m \quad (3)$$

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[1 + 10 \frac{H}{W}\right]^{-0.5} \quad (4)$$

Here  $W$ ,  $Th$ ,  $H$  and  $\epsilon_{eff}$  denote the interconnect width, thickness, height, and effective permittivity, respectively.  $\rho$  is the conductor's resistivity. The coupling capacitance (PUL) for microstrip interconnects can be determined using the following equations [37]:

$$C_c = \frac{\pi \ln\left(1 + \left(\frac{2}{\Delta_{12}}\right)^2\right)}{\frac{1}{4} \left[ \ln\left(1 + \left(\frac{2}{\Delta_{12}}\right)^2\right) \right]^2 - \left[ \ln\left(1 + \frac{4\pi}{\Pi_1}\right) \right]^2} \quad (5)$$

$$\Pi_1 = \epsilon_r P_1 + (1.07(\epsilon_r - 1)^{1.15}) \cdot P_1^{\frac{\beta}{1+1.6P_1}} \quad (6)$$

$$P_1 = \frac{2(W + Th)}{H + \frac{Th}{2} \left(1 - \frac{1}{\epsilon_r}\right)} \quad (7)$$

$$\beta = \ln\left(1.15 + \frac{1.17}{\epsilon_r}\right) \quad (8)$$

$$\Delta_{12} = (3.6 \tanh\{0.09 \cdot (\epsilon_r - 1)\}) \cdot D_{12}^{1.5} + (1 + 0.36 \cdot (\epsilon_r - 1)^{0.65}) \cdot D_{12}^{(\epsilon_r - 0.66)} \quad (9)$$

$$D_{12} = \frac{W + Sp}{H + Th/4} \quad (10)$$

The drivers are modeled with a resistance  $R_d$  and a capacitance  $C_d$  using alpha-power model [38]. The values of these parameters for a minimum size buffer are listed in table 1.

### 3. Study of SL Structures

In this section, the crosstalk voltage and the propagation delay in two structures, consist of partially coupled interconnects with the same length (SL) are evaluated. These structures are illustrated in Fig. 1. The victim line in structure A is placed slightly behind the aggressor line. In contrast, the victim line in structure B is placed slightly ahead of the aggressor line.

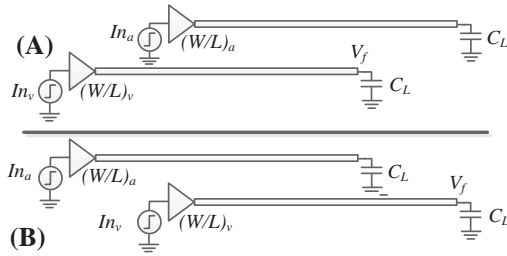


Fig. 1. The structure A and structure B consist of partially coupled identical lines (SL) for studying the crosstalk voltage.

### 3.1. Analytical formulations

In order to model the SL structures in Fig. 1, a simple RC model is used. Based on this model, the interconnects have been divided into two segments: non coupled length which is modeled using lumped RC model (represented by  $R_1$  and  $C_1$ ) and coupled length which is modeled using T model (represented by  $R_2$  and  $C_2$ ) (Fig. 2). The variables  $R_1$ ,  $C_1$ ,  $R_2$ , and  $C_2$  are calculated using (11) to (14). In Fig. 2,  $C_c$  is the coupling capacitance related to the coupled length.  $R_{w1}$ ,  $C_{w1}$  and  $R_{w2}$ ,  $C_{w2}$  represent the wire resistance and wire capacitance of non-coupled length and coupled length, respectively. After writing the KCL equations in the nodes of the equivalent circuit models of the both structures, and performing mathematical calculations, the crosstalk voltage expressions are obtained. Equations (15) to (19) define the crosstalk voltage at the end point of the victim line in structure A, where this line is placed behind the aggressor line. The crosstalk voltage of structure B is determined using (20) to (24). To simplify the crosstalk expression in structure B, the second  $R_2/2$  resistances in the T models are neglected.

$$R_1 = \frac{R_{w1}}{\sqrt{2}} \quad (11)$$

$$C_1 = \frac{C_{w1}}{\sqrt{2}} \quad (12)$$

$$R_2 = R_{w2} \quad (13)$$

$$C_2 = C_{w2} \quad (14)$$

The crosstalk voltage expressions for structure A in SL are derived as follow:

$$V_f = \frac{V_{in} s C_c Z_1}{(1 + s C_c Z_1) \left( 1 + \frac{Z_x}{Z} + \frac{s Z_x C_c}{1 + s C_c Z_1} \right)} \quad (15)$$

$$V_x = \frac{V_{in}}{s R_d C_d + 1} \quad (16)$$

$$Z_1 = \left\{ \left[ (R_n + R_1) \parallel \frac{1}{s C_1} + \frac{R_2}{2} \right] \parallel \frac{1}{s C_2} \right\} \parallel \left( \frac{R_2}{2} + C_L \right) \quad (17)$$

$$Z_x = \frac{R_d + \frac{R_2}{2} + s \frac{R_2}{2} R_d C_d}{s R_d C_d + 1} \quad (18)$$

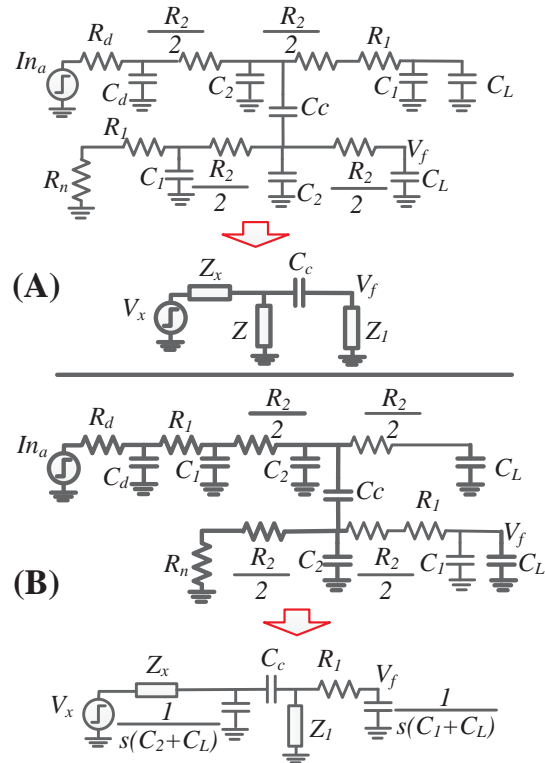


Fig. 2. The circuit model of the structures A and B of SL.

$$Z = \frac{s \left( \frac{R_2}{2} + R_1 \right) (C_1 + C_L) + 1}{s^2 C_2 \left( \frac{R_2}{2} + R_1 \right) (C_1 + C_L) + s (C_2 + C_1 + C_L)} \quad (19)$$

The crosstalk voltage expressions for structure B in SL are derived as follow:

$$V_f = \frac{V_x}{(1 + s R_1 (C_1 + C_L)) (M)} \quad (20)$$

$$V_x = \frac{V_{in}}{(1 + s R_1 C_1) \left( 1 + s R_d C_d + \frac{s R_d C_1}{1 + s R_1 C_1} \right)} \quad (21)$$

$$M = \left( \frac{1 + s C_c Z_1}{s C_c Z_1} + \frac{C_1 + C_L}{C_c + s C_c R_1 (C_1 + C_L)} \right) \times \left( 1 + s Z_x (C_2 + C_L) \right) + \frac{Z_x}{Z_1} + \frac{s Z_x (C_1 + C_L)}{1 + s R_1 (C_1 + C_L)} \quad (22)$$

$$Z_1 = \frac{R_n + \frac{R_2}{2}}{s (R_n + \frac{R_2}{2}) (C_1) + 1} \quad (23)$$

$$Z_x = \frac{R_d + R_1 + s R_1 R_d R_d}{s^2 R_1 R_d C_d C_1 + s (R_d C_d + R_1 C_1 + R_d C_1) + 1 + \frac{R_2}{2}} \quad (24)$$

By substituting the values of the parameters from TABLE I into (15) and (20), the crosstalk voltage waveforms can be calculated (Fig. 3). The crosstalk

voltage waveforms, obtained using HSPICE simulations are demonstrated in Fig. 4. The comparison between the simulation and analytical results of the crosstalk voltage are brought in Table 2.

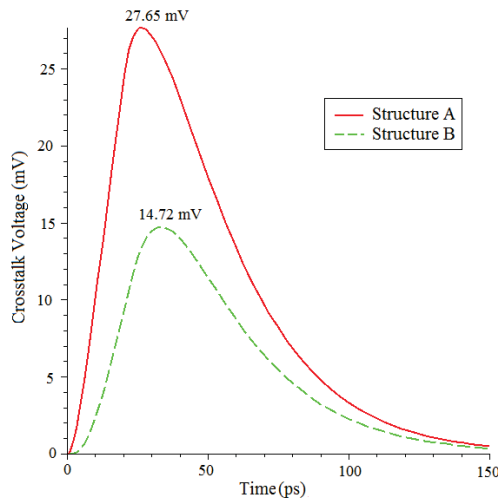


Fig. 3. Crosstalk voltage waveforms in SL structures obtained from the analytical expressions.

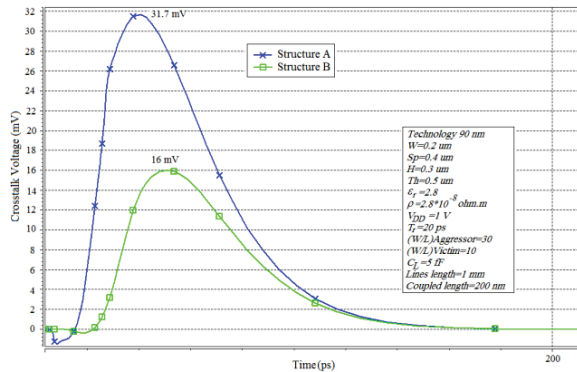


Fig. 4. The crosstalk voltage waveforms from HSPICE simulations of structures A and B in SL.

table 2. Maximum crosstalk noise in the structures of SL, obtained analytically and by simulation.

Victim placement	Crosstalk Voltage (mV)		
	Analytical model	HSPICE	Error %
A (victim is behind)	27.65	31.7	12.8
B (victim is ahead)	14.72	16	8
Relative difference ( $ A-B  \times 100/B$ )	87.8%	98.1%	
Error = $ Model - HSPICE  \times 100/HSPICE$			

## 3.2. Comprehensive crosstalk study of the SL structures

In this section, we attempt to study the crosstalk voltage and delay variations in SL structures when changing different individual parameters. A simple expression for the crosstalk peak voltage can be used to investigate the crosstalk noise and the delay variations. The crosstalk peak voltage  $V_p$  can be expressed with the following equations [39]:

$$V_p = \frac{C_c}{C_c + C_{wT}} \times \frac{V_{DD}}{1 + \frac{\tau_a}{\tau_v}} \quad (25)$$

$$\tau_a = R_d(C_d + C_{wa} + C_{La} + C_c) \quad (26)$$

$$\tau_v = R_n(C_{wv} + C_{Lv} + C_c). \quad (27)$$

Here  $C_{wT} = C_{wv} + C_{Lv}$  while  $C_L$  and  $C_w$  are the load capacitance and the wire capacitance, respectively. Subscripts "a" and "v" refer to the aggressor line and the victim line, respectively. In the rest of this section, we consider several parameters and study the variations of crosstalk voltage.

### 3.2.1. Coupled length

Regarding to individual variation of parameters, initially, the coupled length is increased from minimum coupling length (0.1mm) to almost full-length coupling (1.9mm), while the wires lengths are kept at 2mm. The waveforms of the crosstalk voltage and the propagation delay of structures A and B are shown in figures 5 and 6.

It is observed from the figures that for both structures, the longer the coupled length gets, the higher the crosstalk peak voltage becomes. At the minimum and maximum coupled lengths, structures A and B have almost the same crosstalk amplitude, because at the beginning it can be assumed that both structures have no coupling and the aggressor and victim lines do not have overlap. For the maximum value they have almost complete coupling and so the shape and the crosstalk of structure A will be similar to that of structure B. In

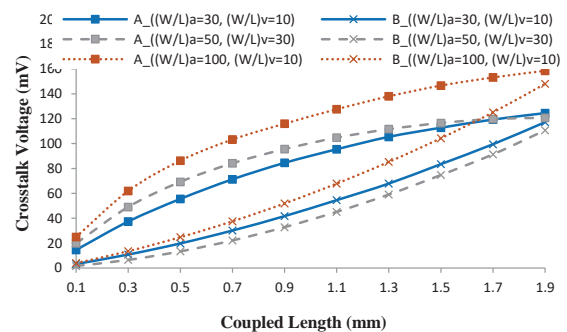


Fig. 5. The crosstalk voltage of structures A and B in SL versus the coupled length (Wires length=2mm).



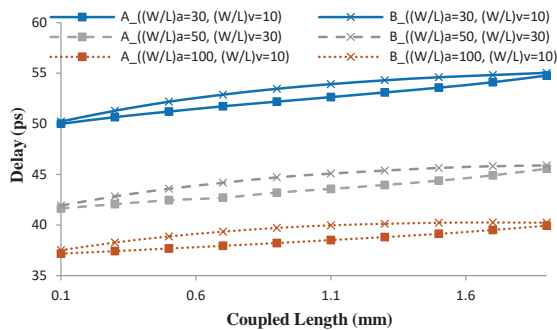


Fig. 6. The delay of structures A and B in SL versus the coupled length (Wires length=2mm).

contrast to the minimum and maximum coupling length, in the middle, there is a specific length where the discrepancy between the crosstalk voltage of structures A and B gets maximum. The delay of SL structures increases, while the delay in structure B is always more than structure A.

When the coupled length in SL structures increases, the coupling capacitance  $C_c$  increases as well and according to (25) it causes the crosstalk amplitude to rise. Since the propagation delay is measured at the end of the aggressor line, due to the increase in the total capacitance of this wire, the delay of both structures will slightly rise.

At this point, we intend to study another situation for crosstalk evaluation in SL case study. As such, firstly, structure A is considered at initial point where the coupled length equals to 0.1mm. Then, the victim line is thoroughly moved forward until a full coupling (2mm) is reached. Thereafter, the forward moving is continued until the final position of structure B, i.e., 0.1mm overlaps is reached. Fig. 7 shows the crosstalk peak voltage versus the distance between the outputs of the aggressor driver and the victim line (0.1mm to 3.9mm). It is clear that the crosstalk peak voltage, first rises and then after the maximum value, it starts to decline due to a decrease in the coupled length.

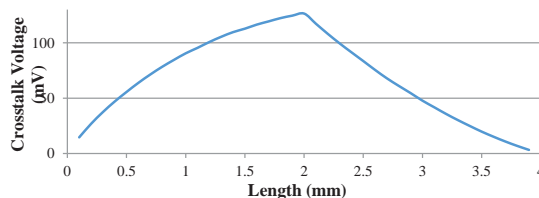


Fig. 7. The crosstalk voltage in SL structures, versus the position of the victim line, when it moves from behind the aggressor line to ahead of it.

### 3.2.2. Line length

As the wires lengths in SL are increased (assuming the coupled length equal to constant value 0.5mm), the crosstalk voltage in both structures declines. However, since the waveform of structure A doesn't drop as sharp as structure B, it shows that structure A has less sensitivity to this parameter. The aggressor lines delays the line length (Coupled length=0.5mm).

of the two structures are almost the same and both soar as the lines lengths increase. The crosstalk voltage and the delay waveforms of SL structures versus this parameter are illustrated in figures 8 and 9, respectively.

Since the coupled length remains constant, the capacitance  $C_c$  in (25) doesn't change although  $\tau_a$ ,  $\tau_v$  and  $C_{wT}$  increase. Increasing these parameters cause the crosstalk voltage in both SL structures to decline. In structure A, the distance between the outputs of the aggressor driver and the victim line (where crosstalk is measured) doesn't change. In structure B this distance varies as the lines lengthen. Hence, the variation of this length has a larger effect on the crosstalk voltage of structure B rather than structure A. The delay is related to the aggressor line. Lengthening the aggressor lines leads to an increase in the delay of both SL structures.

In SL, if the victim driver gets larger than a specific size, crosstalk voltage of structure A will slightly increase unlike the other cases in Fig. 8. For long lengths, the size of the victim driver doesn't have a considerable influence on the amplitude of the crosstalk voltage. In contrast, for short lengths, if the victim driver gets larger its resistance becomes smaller. This decrease in the resistance value, cause the crosstalk peak voltage to decline. Therefore, when the lines lengthen, the crosstalk voltage should slightly rise in order to reach the final value.

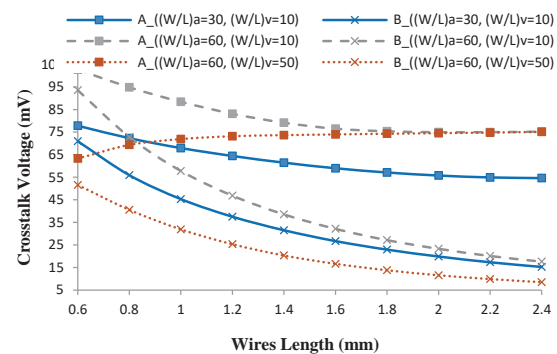


Fig.8.The crosstalk voltage of structures A and B in SL versus the line length (Coupled length=0.5mm).

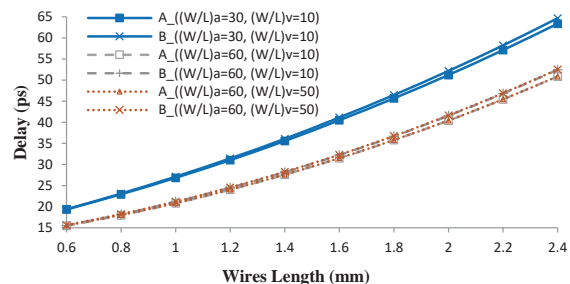


Fig. 9. The delay aggressor lines of structures A and B in SL (versus

table. 3. The manner of wires figurative changes during length variations.

Variable	Structure	A	B
Wire length	SL		
Coupled length	SL		

The manner of the SL structures figurative changes, during the coupled lengths and the wires lengths increase, are illustrated in table 3.

### 3.2.3. Aggressor driver size

When the driver size of aggressors, in both SL structures, get larger, they become stronger and transfer the signals with less delay. According to (26), an increase in size of this driver causes a decrease in  $\tau_a$ ; thus, the crosstalk amplitude rises (Fig. 10). As this driver gets larger, the difference between the crosstalk voltages of the two structures will increase. This can be explained by the fact that the aggressor driver in structure A is closer to the coupling region and affects the crosstalk amplitude of structure A more than that of structure B.

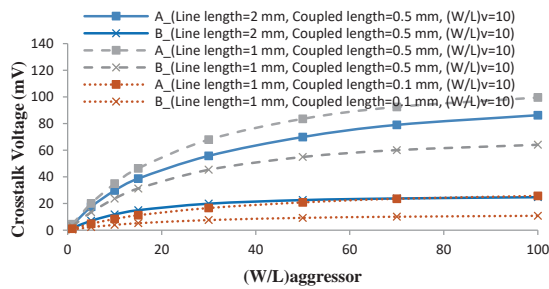


Fig. 10. The crosstalk voltage of structures A and B in SL versus the aggressor driver size.

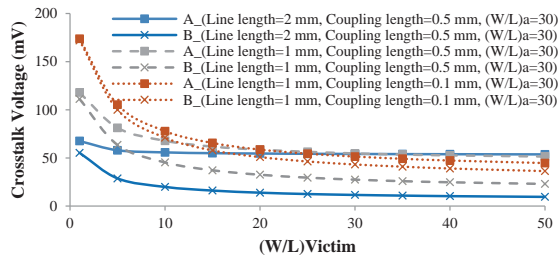


Fig. 11. The crosstalk voltage of structures A and B in SL versus the victim driver size.

### 3.2.4. Victim Driver Size

As discussed earlier, due to the constant victim input signal, only the NMOS transistor of the driver will be on and can be modeled with a resistance  $R_n$ . This resistance becomes smaller as the victim driver size gets larger. If  $R_n$  in (27) decreases,  $\tau_v$  will decline and according to (25) the crosstalk voltage gets smaller (Fig. 11). In structure B,  $R_n$  is close to the coupling region and as this resistance gets smaller, the crosstalk peak voltage decreases more dramatically. That's the

reason why crosstalk voltage in structure B drops more considerably than in structure A.

### 3.2.5. Load Capacitance

When the load capacitance  $C_L$  of the aggressor line rises,  $\tau_a$  in (39) increases as well. This causes the crosstalk voltage waveform of both structures to drop (Fig.12). Increasing the victim load capacitance increases  $\tau_v$  in (27) and  $C_{wT}$  in (25) which causes a decrease in the crosstalk amplitude (Fig. 13). If the load capacitances of both lines get larger, the changes in  $\tau_a$  and  $\tau_v$  will be similar; hence, the variation in their ratio can be neglected. However, increasing  $C_{wT}=C_{wv}+C_{Lv}$ , causes the crosstalk voltage in both structures to decline (Fig. 14).

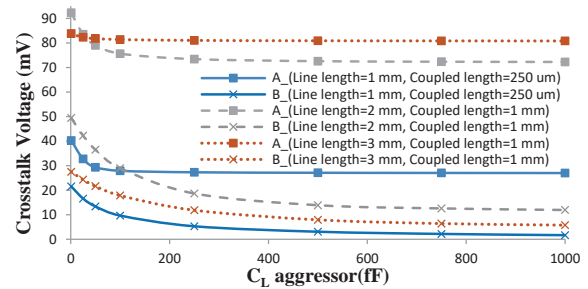


Fig. 12. The crosstalk voltage of structures A and B in SL versus the aggressor load capacitance ((W/L)<sub>a</sub>=30, (W/L)<sub>v</sub>=10).

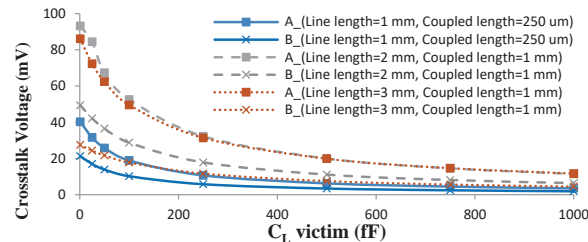


Fig. 13. The crosstalk voltage of structures A and B in SL versus the victim load capacitance ((W/L)<sub>a</sub>=30, (W/L)<sub>v</sub>=10).

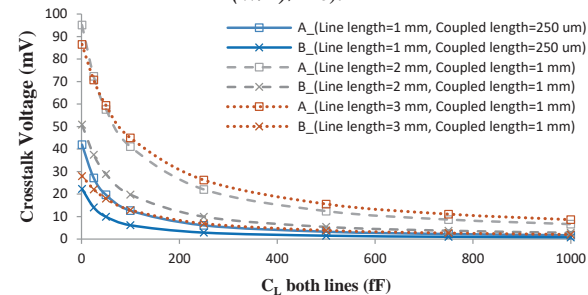


Fig. 14. The crosstalk voltage of structures A and B in SL versus the load capacitances ((W/L)<sub>a</sub>=30, (W/L)<sub>v</sub>=10).

### 3.3. Multiple Change of Parameters

In the preceding section, the influence of each parameter variation on the crosstalk voltage amplitude in SL structures was evaluated individually. Accordingly, all the figures 5 to 14 show the corresponding results. Now we integrate our new results for the crosstalk amplitude variations while the values of the aggressor driver size, the victim driver size, the wires lengths, and the coupled length are varied.

Fig. 15 demonstrates the crosstalk voltage of structures A and B, and the difference between them. In order to study the effect of the length parameter, the lines lengths are assumed to be 1mm and 2mm. For each line length, the coupled length is set to  $\frac{1}{4}$  and  $\frac{3}{4}$  of the total line length which leads to four cases. For each of them, the victim driver size is assumed to be 1 and 10, and finally for each of these eight cases the aggressor driver size increases from 10 to 100. From Fig. 15 it can be understood that the crosstalk voltages,

for each couple of precisely corresponding measurements in 1mm and 2mm length situations, are roughly the same due to the increase of all lengths. Both the wires and the coupled region double in length, as a result their effects on the amplitude of the crosstalk voltage remain almost unchanged. It can be observed that by increasing the size of the aggressor driver, the crosstalk voltage in both structures and also their discrepancy rise. If the victim driver gets larger, the crosstalk amplitude drops while the difference between the crosstalk voltages of the two structures increases.

Fig. 16 shows the propagation delay of both structures and their difference. It can be inferred that the delay declines as the aggressor driver size increases. The delay discrepancy between structures A and B can be ignored. When the lines lengths equal to 2mm, the delays of all cases become two times more than the exact corresponding measurements in the four cases when the lines lengths are 1mm

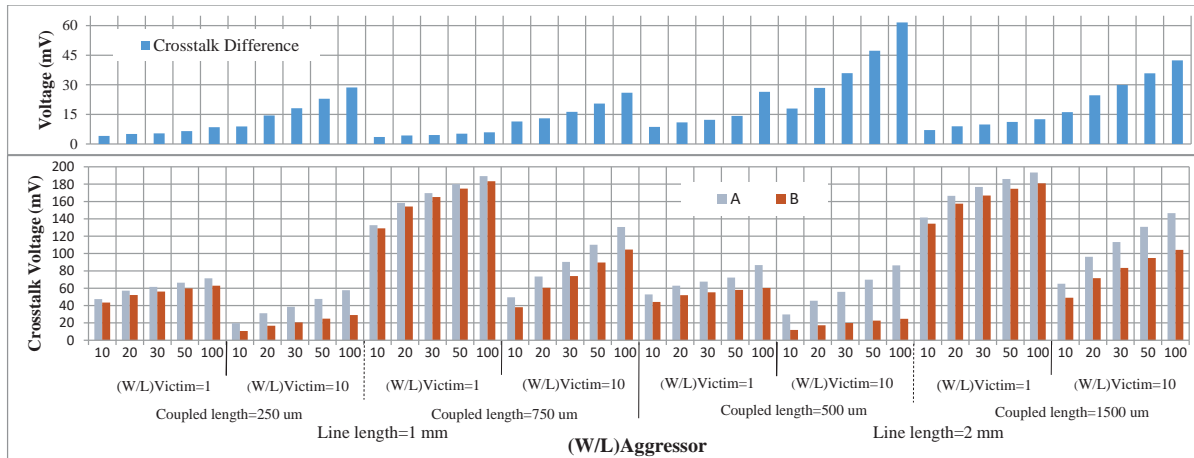


Fig. 15. The crosstalk voltage of structures A and B in SL versus the variation of different parameters (lower diagram) and the difference between them (upper diagram).

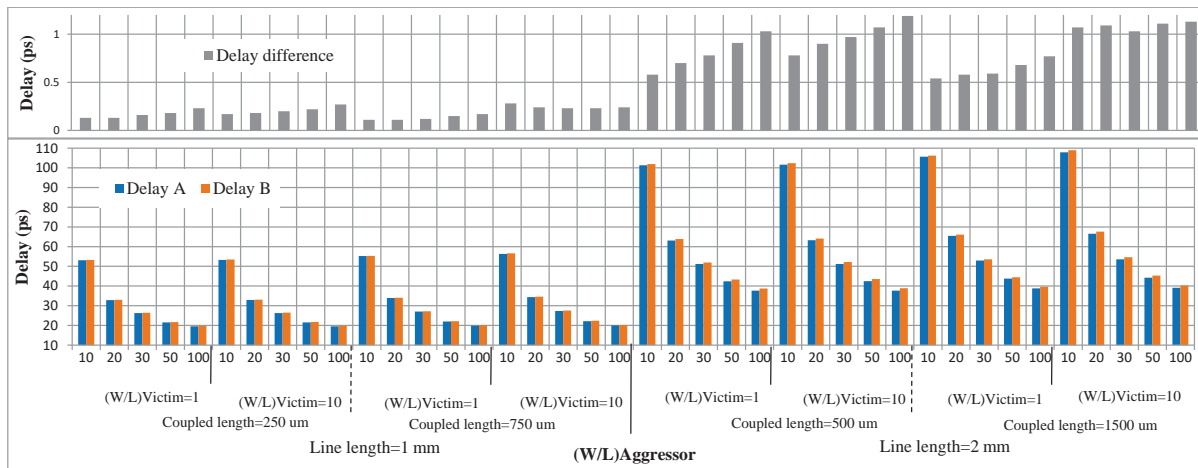


Fig. 16. The delay of structures A and B in SL versus the variation of different parameters (lower diagram) and the difference between them (upper diagram).



**Table 4. Variations of the crosstalk and delay in structures of SL for changing different parameters.**


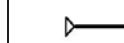



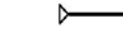

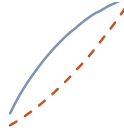
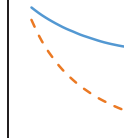
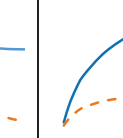
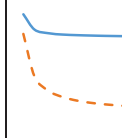
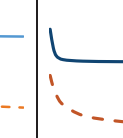
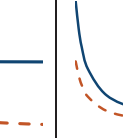
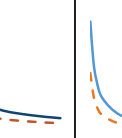
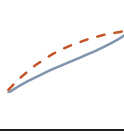
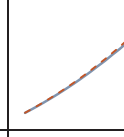
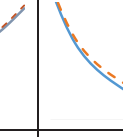
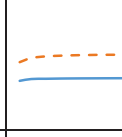



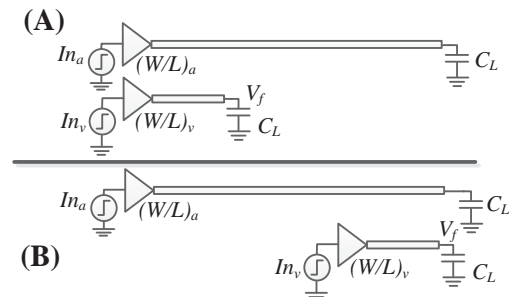
	Structure A			Structure B			
							
Crosstalk Voltage							
Delay							
Variable (increasing)	Coupled length	Wires length	Aggressor driver	Victim driver	Aggressor capacitance	Victim capacitance	Both lines capacitances

Table 4 shows the form of changes in the crosstalk voltage and the delay of the SL structures, according to the variations of different parameters.

#### 4. Study of LA\_SHV Structures

The second case which we report the results of investigation in this article, is called LA\_SHV. It consists of a long aggressor line and a short victim line. This group of structures is illustrated in Fig.17. The victim line in structure A is placed at the beginning of the aggressor line, and in structure B it is placed at the end of the aggressor line.

**Fig. 17. The structures A and B with different lengths (LA\_SHV) for studying the crosstalk voltage.**

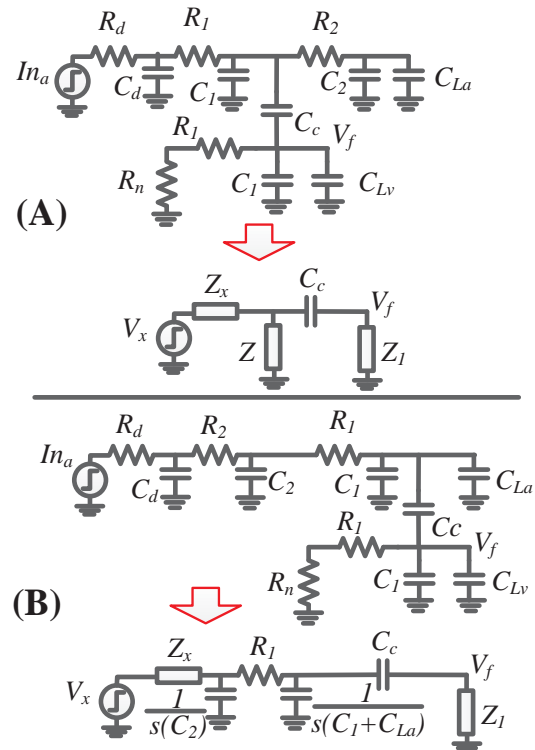
##### 4.1. Analytical formulations

LA\_SHV structures are modeled using lumped RC networks (Fig. 18). In this figure,  $R_1$  and  $C_1$  represent the resistance and the capacitance of the coupled region which is equal to the length of the victim line.  $R_2$  and  $C_2$  represent the resistance and the capacitance of non-coupling region. These parameters can be calculated using (28) to (31). In these expressions,  $R_w$  and  $C_w$  denote the resistance and the capacitance of the related wire length.

$$R_1 = \frac{R_{w1}}{\sqrt{2}} \quad (28)$$

$$C_1 = \frac{C_{w1}}{\sqrt{2}} \quad (29)$$

$$R_2 = \frac{R_{w2}}{\sqrt{2}} \quad (30)$$

**Fig. 18. Circuit models for the structures LA\_SHV.**

$$C_2 = \frac{C_{w2}}{\sqrt{2}} \quad (31)$$

After writing the KCL equations for all nodes of the circuit model in both structures, and using mathematical calculations, the crosstalk voltage at the end of the victim line in both structures of LA\_SHV can be calculated.

The crosstalk voltage of structure A in LA\_SHV is given by:

$$V_f = \frac{V_{in} \cdot Z_1}{(1 + sR_d C_d) \left( Z_1 + \frac{1}{sC_c} \right) \left( \frac{Z_x}{Z} + \frac{Z_x}{Z_1 + \frac{1}{sC_c}} + 1 \right)} \quad (32)$$

$$Z_x = \frac{R_d + sR_1R_dC_d + R_1}{1 + sR_dC_d} \quad (33)$$

$$Z_1 = \frac{R_n + R_1}{1 + s(R_n + R_1)(C_1 + C_{Lv})} \quad (34)$$

$$Z = \frac{1 + sR_2(C_2 + C_{La})}{s^2C_1R_2(C_2 + C_{La})} \quad (35)$$

The crosstalk voltage of structure B in LA\_SHV is given by:

$$V_f = \frac{V_x(sZC_c)}{\left(1 + s(M) + s^2R_1Z_xC_2\left(C_1 + C_{La} + \frac{C_c}{1 + sZC_c}\right)\right)} \times \frac{1}{(1 + sZC_c)} \quad (36)$$

$$M = (C_1 + C_{La})(Z_x + R_1) + \frac{C_c(Z_x + R_1)}{1 + sZC_c} + Z_xC_2 \quad (37)$$

$$Z_x = \frac{R_d + R_2 + sR_2R_dC_d}{1 + sR_dC_d} \quad (38)$$

$$Z_1 = \frac{R_n + R_1}{1 + s(R_n + R_1)(C_1 + C_{Lv})} \quad (39)$$

$$V_x = \frac{V_{in}}{1 + sR_dC_d} \quad (40)$$

Figures 19 and 20 show the crosstalk voltage of both structures, obtained analytically and by simulations respectively, when the values of table 1 substitute the corresponding parameters of the equations. As it is observed in table 4, the obtained results from the analytical model and the HSPICE simulations are almost similar, and the difference is because of using a simple model for comparing two structures rather than a complicated one.

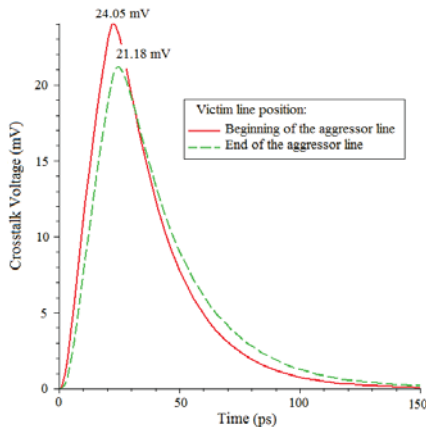


Fig.19. Crosstalk waveforms in LA\_SHV obtained from the analytical expressions.

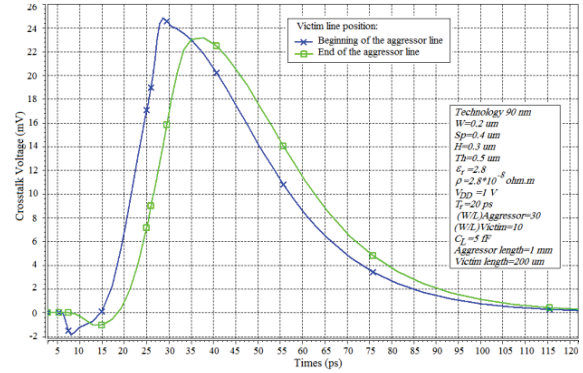


Fig. 20. The waveforms from HSPICE simulations of structures A and B in LA\_SHV.

Table. 5. Maximum crosstalk noise in the structures of LA\_SHV, obtained analytically and by simulation.

Victim placement	Crosstalk Voltage (mV)		
	Analytical model	HSPICE	Error*
Structure (A)	24.05	24.86	3.2 %
Structure (B)	21.18	23.17	8.6%
Relative difference ( A-B ×100/B)	13.5%	7.3%	

\*: Error = |Model – HSPICE|×100/HSPICE

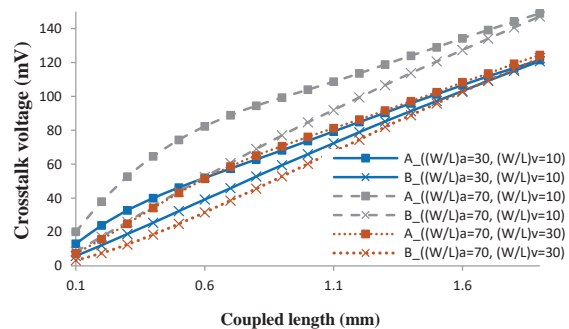
## 4.2. Comprehensive crosstalk study of the LA\_SHV structures

In this section each circuit parameter is varied individually in order to study its effects on the crosstalk voltage and the delay in the LA\_SHV structures. As explained in Section III, using a simple expression for crosstalk voltage such as (25) would help to understand the manner of crosstalk voltage variations more easily. Next, different parameters are varied and their effects on the crosstalk voltage amplitude are investigated.

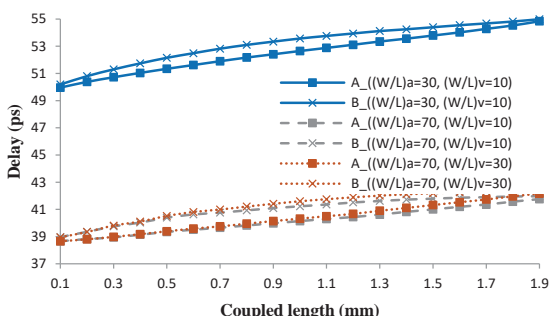
### 4.2.1. Coupled length

Increasing the coupled length means increasing the victim wire length. Figures 21 and 22 show the variations of the crosstalk voltage and the delay, respectively, when the coupled length increases from 0.1mm to almost full-length coupling, 1.9mm.

Lengthening the victim line increases the coupling capacitance  $C_c$  and causes the crosstalk voltage in both structures to rise. Due to the structures similarity, in the case of full-length coupling the crosstalk peak voltage of the two structures will have the same value.



**Fig. 21. The crosstalk voltage of structures A and B in LA\_SHV versus the coupled length (Aggressor length=2mm).**



**Fig. 22. The delay of structures A and B in LA\_SHV versus the coupled length (Aggressor length=2mm).**

#### 4.2.2. Line Length

In this case, the line length represents the aggressor length. If the aggressor length increases (while the coupled length is assumed to be 0.2mm), the crosstalk voltage in both structures declines while the delay rises dramatically. The variations of these two parameters versus the aggressor length are illustrated in the figures 23 and 24. Since the coupled length remains constant,  $C_c$  doesn't change in (25), but an increase in the value of  $\tau_a$  causes the crosstalk voltage in both structures to fall. In structure A, the distance between the outputs of the aggressor driver and the victim line (where crosstalk is measured) doesn't change. In structure B this distance increases as the aggressor wire lengthens. Thus, variations of this length affect the crosstalk voltage of structure B more than that of structure A. The propagation delay is solely related to the aggressor line. Making this line longer, cause the delay of both structures to increase.

The decrease in the crosstalk voltage in structure A in LA\_SHV stops after a specific length and the crosstalk voltage amplitude remains constant. The reason behind this phenomenon backs to the impedance of the aggressor line. If the aggressor line gets longer, its equivalent line capacitance and resistance will become larger as well, but the equivalent impedance approaches almost a constant amount.

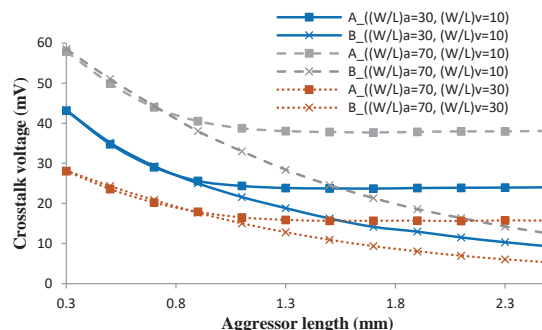
The manner of the structures figurative changes, during the increase of the victim length and the aggressor length are illustrated in table 6.

**Table 6. The manner of wires figurative changes during length variations**

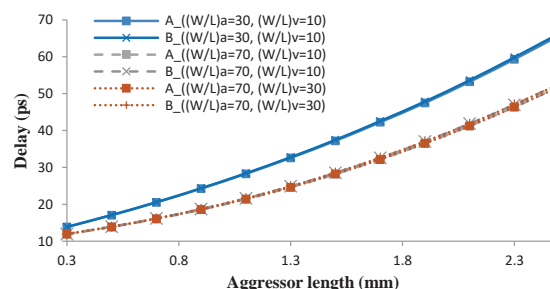
Variable	A	B
Victim length		
Aggressor length		

#### 4.2.3. Aggressor Driver Size

When the aggressor driver gets larger, it becomes stronger and transfers the signals with less delay. Consequently, similar to the SL structures, the crosstalk amplitude in both structures increases (Fig. 25).



**Fig. 23. The crosstalk voltage of structures A and B in LA\_SHV versus the aggressor length (Victim length=0.2mm).**



**Fig. 24. The delay of structures A and B in LA\_SHV versus the aggressor length (Victim length=0.2mm).**

#### 4.2.4. Victim Driver Size

Increasing the victim driver size decreases the equivalent transistor resistance  $R_n$ . Due to the increase in  $\tau_v$  the crosstalk peak voltage in (38) decreases. The crosstalk voltage of LA\_SHV structures versus the victim driver size are shown in Fig. 26.

#### 4.2.5. Load capacitance

In this part, the aggressor load capacitance the victim load capacitance, and the load capacitances of both lines are varied and their effects on the crosstalk voltage are investigated. The results for these three cases are illustrated in the figures 27 to 29. In the three mentioned cases, increasing the load capacitance leads to a drop in the crosstalk voltage of the structures A and B.

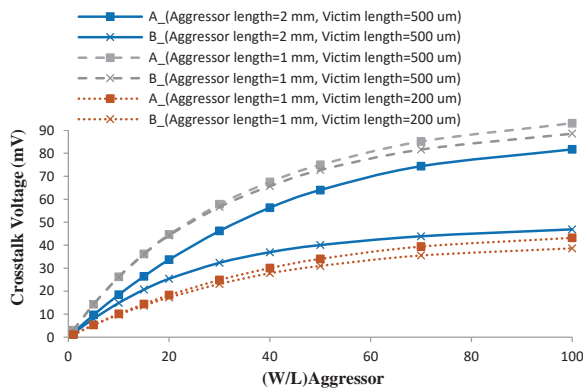


Fig. 25. The crosstalk voltage of structures A and B in LA\_SHV versus the aggressor driver size (when lines lengths change and victim driver=10).

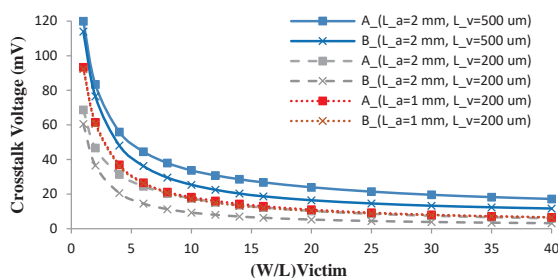


Fig. 26. The crosstalk voltage of structures A and B in LA\_SHV versus the victim driver size (when lines lengths change and aggressor driver =20).

### 4.3. Multiple Change of Parameters

In this section, the results for changing multiple parameters are gathered and integrated to explore new achievements. For this purpose, the values of the aggressor driver size, the victim driver size and the aggressor length are considered.

Fig. 30 shows the crosstalk voltage of the structures A and B, and their discrepancy. In order to study the effect of length parameter, the aggressor length is assumed to be 1mm and 2mm, while the victim length

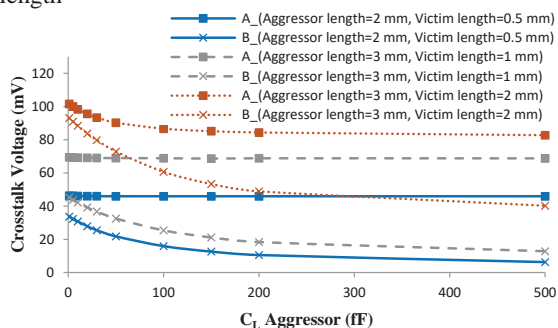


Fig. 27. The crosstalk voltage of structures A and B in LA\_SHV versus the load capacitances of the aggressor lines ((W/L)<sub>a</sub>=30, (W/L)<sub>v</sub>=10).

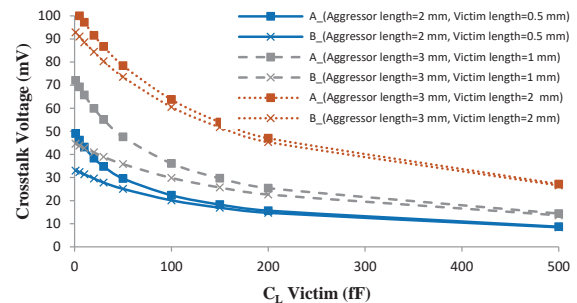


Fig.28. The crosstalk voltage of structures A and B in LA\_SHV versus the load capacitances of the victim lines ((W/L)<sub>a</sub>=30, (W/L)<sub>v</sub>=10).

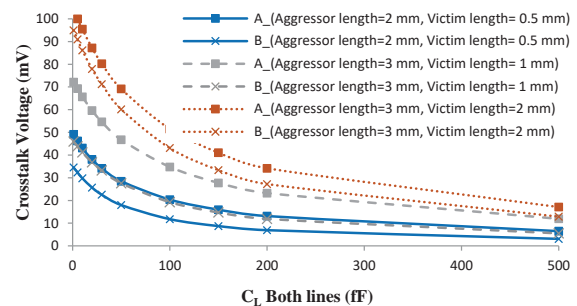


Fig.29. The crosstalk voltage of structures A and B in LA\_SHV versus the load capacitances of both lines ((W/L)<sub>a</sub>=30, (W/L)<sub>v</sub>=10).

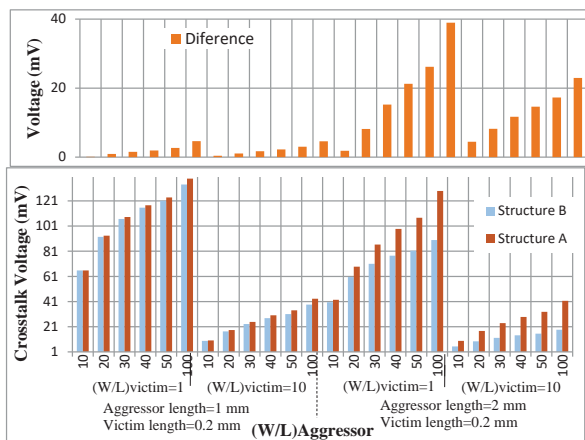
is constant with the value of 0.2mm. For each of these two cases, the victim driver size is assumed to be 1 and 10. Finally, for each of these four cases, the aggressor driver size varies between 10 and 100. As can be seen in this figure, increasing the size of the aggressor driver raises the crosstalk voltage in both structures and also their difference. If the victim driver gets larger, the crosstalk voltage amplitude drops.

Fig. 31 demonstrates the delay of both structures and their difference. It is inferred that the propagation delay declines as the aggressor driver size increases. The difference of the delay between the structures A and B can be neglected. When the lines lengths get equal to 2mm, the delays amplitudes are approximately two times larger than the exactly corresponding measurements in the two cases when the lines lengths were 1mm.

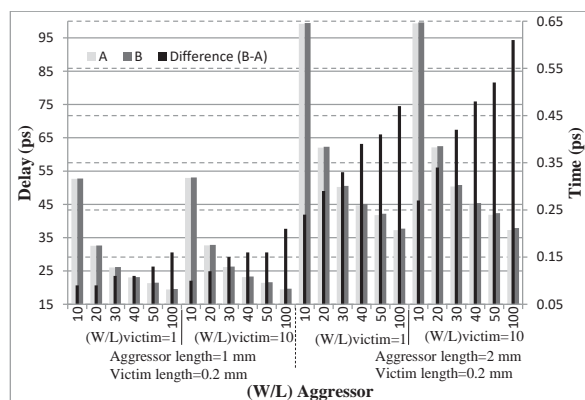
Table.7. illustrates the form of variations in the crosstalk voltage and the delay of the LA\_SHV structures, according to increase of different parameters.

## 5. Conclusion

In this research, we have attempted to analyze and explore variations and the form of the crosstalk voltage and the delay relative to the change of different circuit parameters in two groups of structures named SL and LA\_SHV. The main objective of this work was investigating the structures, consisting of coupled parallel interconnects with partially coupling and/or different lengths.



**Fig. 30.** The crosstalk voltage of structures A and B in LA\_SHV for change of different parameters (lower diagram) and the difference between them (upper diagram).



**Fig. 31.** Delay of structures A and B in LA\_SHV for change of different parameters (the left axis) and the difference between them (the right axis).

The methodology used, was to achieve how the crosstalk voltage changes when different parameters are changed while different structures are compared. Initially, the analytical expressions were extracted. Next, different parameters in the two case studies were varied individually or considered together and the shape of the crosstalk noise and the propagation delay variations have been extracted and evaluated. It was shown that by optimizing the parameters, the crosstalk voltage in B structures in SL and LA\_SHV varies 1%-92% and 0%-86%, respectively, less than A structures of the two groups. Moreover, this study demonstrates that, the closer the aggressor driver gets to the end of the victim line and the place of measurements, the more the crosstalk voltage increases.

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**Table 7.** Variations of the crosstalk and delay in structures of LA\_SHV for changing different parameters.

	Structure A			Structure B			
<b>Crosstalk Voltage</b>							
<b>Delay</b>							
<b>Variable (increasing)</b>	Victim length	Aggressor length	Aggressor driver	Victim driver	Aggressor capacitance	Victim capacitance	Both lines capacitance

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