A Broadband Low Power CMOS LNA for 3.1–10.6 GHz UWB Receivers

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Abstract:

A new approach for designing an ultra wideband (UWB) CMOS low noise amplifier (LNA) is presented. The aim of this design is to achieve a low noise figure, reasonable power gain and low power consumption in 3.1-10.6 GHz. Also, the figure of merit (FOM) is significantly improved at 180nm technology compared to the other state-of-the-art designs. Improved π-network and T-network are used to obtain a high and smooth power gain for the whole frequency band. Impedance matching and noise matching are designed with double feedback and only one inductor that are used at the input of the LNA. Post layout simulation is done for design validation. In this design post layout simulations show the low noise figure of 3.85±0.25 dB, reasonable power gain (18.08dB) and input return loss less than -9.1dB in full band of UWB. The power consumption of the circuit is only 11.3mW from 1.8V voltage supply. The LNA has the group delay about 111±43ps. An input third-order intermodulation point (IIP3) of -9.2 dBm is achieved at 4 GHz. The layout area is 1.056×0.658 mm^2.

Keywords: Ultra wideband, UWB, Low Noise Amplifier, LNA, CMOS.

Submission date: 30, April,2015

Conditionally accepted date: 5, Sep., 2015

Acceptance date: 19, Sep., 2016

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1. Introduction

Applications of UWB communication in short-range and high speed mobile systems have been popular in academic and industry due to commercialization of the frequency band of 3.1GHz to 10.6GHz by Federal Communications Commission (FCC) in 2002 [1]. Since, then there have been many researches on UWB.

Two methods have been introduced to use the UWB spectrum, i.e. Frequency hopping (FH) scheme [2] and impulse radio (IR)[3]. In frequency hopping scheme, the UWB band (3.1-10.6 GHz) is divided to fourteen 528 MHz sub bands with OFDM modulation. In impulse radio, transmission of very short pulses is used with pulse position or polarity modulation.

It is possible to have data rates up to 480Mbps in the lower band of UWB (3.1-4.8GHz). Higher data rates can be obtained by using upper band of the UWB. Fig. 1 shows the lower band and upper band of UWB which consists of band group 1 and 3-5 respectively.

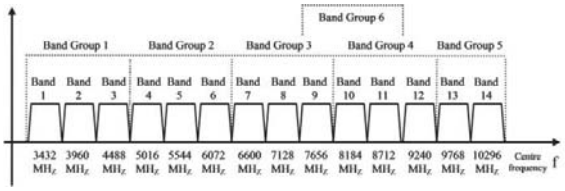


Fig.1. Band group and frequency limit of UWB

An ultra wideband (UWB) low noise amplifier (LNA) for a wireless front-end is crucial in a wide range of receiver architectures. The amplifier must meet several stringent requirements, such as broadband input matching to minimize the return loss, sufficient gain to suppress the noise of a mixer, noise match to achieve low noise figure (NF) and enhance receiver sensitivity, low power consumption to increase battery life, high linearity to have high dynamic range and low output intermodulation distortion in high power input and small die area to reduce the cost.

The paper is organized as follows. Section 2 describes the recent design of common ultra wideband LNA topologies, namely, common-gate, resistive shunt feedback, distributed amplifier and current reuse. Section 3 introduces the widening technique and noise-canceling followed by the proposed circuit topology. In Section 4, analytical equations are derived to show the gain performance. In Section 5, the noise analysis, considering the NF at all frequencies is coming. Circuit design and post layout simulation results for proposed ultra wideband LNA are reported in Section 6. Finally, Section 7 presents the conclusion.

2. Recent Research

Different topology of ultra wideband (UWB) CMOS low noise amplifiers (LNAs) have been proposed in literatures in the last decade: e.g. distributed amplifiers [4] (DAs) provide good impedance matching, flat gain and good group delay over a wide range of frequency and excellent IIP3. However distributed amplifiers tend to consume large dc current due to the distribution of multiple amplifying stages, which makes them less attractive for low power application. Also, their demand for high quality transmission lines make them unsuitable for low cost application due to the large silicon area they need. Another topology is resistive shunt feedback architecture proposed by [5] and [6] that provides good wideband matching, higher stability, sufficient linearity and flat gain but tend to suffer from poor noise figure, large power dissipation and insufficient power gain. Alternatively, a reactive feedback implementation provides better noise performance. The common gate configuration [6] uses the resistive part looking into the source of the transistor to match the input to well-defined source impedance (e.g. 50Ω). This topology has the benefit of wide bandwidth, good input-output isolation and linearity, generally independent NF from angular frequency over the bandwidth and wideband input matching. However, for an input of 50Ω, the required input transconductance must be 20mS, which translates into high power consumption. The common gate with the input matching filter topology can solve this problem and achieve better wideband property. The other structure is inductor source degenerated [7] that employs inductor at source terminal to generate a real term for the input impedance and often works with cascode transistor. This method due to its good noise performance, high gain and high reverse isolation, it is usually used in narrowband scheme. Wide band input matching is reported with adapting a band pass LC filter at the input of the inductor source degenerated LNA [8]. The band pass filter incorporates the input impedance of the cascode as a part of the filter and shows good performance while dissipating small amount of dc power. However, the LC filter mandates a number of reactive elements, which could lead to a larger chip area and NF degradation due to low Quality factor of inductors of LC filter. In this method on-chip transformer matching could save some area [9]. Differential amplifiers show excellent treatment toward second order harmonics. These LNAs, however consume extra power likely about two times of their single-ended counterpart [10]. Current reuse technique has been used in many recent LNA topologies to reduce power dissipation especially in mobile devices [11]. This topology composed of two common source configuration stages under common current structure. This method effectively save power but its chip area is large due to using several inductors. Another solution for UWB LNA is to use forward body biasing for reducing threshold voltage of CMOS transistor [12]. This technique needs low voltage supply; its power consumption is very low and is very suitable for low power application. However, using resistor in body terminal for limiting the current makes poor noise performance and the linearity of this method is slightly worse than that of the other designs.

In this work, we propose a figure of merit (FOM) which takes into account power consumption, noise figure, power gain and bandwidth. Due to the input inductor and the double feedback at input, reasonable input impedance and noise matching could be achieved at all over the UWB frequencies. Middle stage could be used for bandwidth gain improvement. Output impedance matching is done with buffer stage. It matches the circuit with standard 50 Ω resistor. Moreover, the high frequency noise can be effectively suppressed by the good noise match at input transistor with size of transistor, input inductor and double feedback network. This leads to proper noise figure. The cascode topology results in good isolation of output from input and has a wideband behavior.

3. Circuit Analysis

Fig. 2 shows a typical narrowband cascode LNA topology with inductive source degeneration. In this topology, the inductors L_s and L_g are added for simultaneous noise matching and input impedance matching. [13].

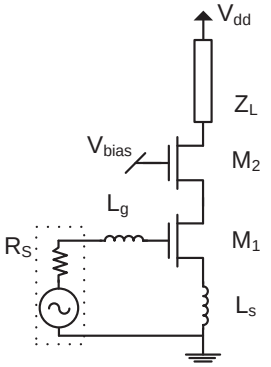
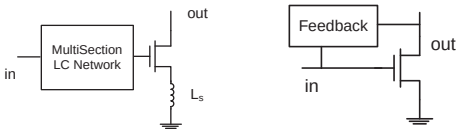


Fig. 2. Narrowband Cascode Source Degenerated LNA Topology

Widening the bandwidth and wideband impedance and noise matching with the source-degenerated UWB CMOS LNA topology can be done in several ways. Fig. 3 shows the multi-section LC network and feedback solution.



(a) **(b)**

Fig. 3. (a) Multisection LC network for wideband input matching (b) Feedback network for wideband input matching

In LC network, overall imaginary input reactance resonates over the bandwidth. In [7] two section on-chip LC chebyshev filter for ultra wideband impedance matching is used. In [14] and [8] a three and two section LC filter is used as input reactive network, respectively. A drawback of this approach for UWB LNA is the large group delay variation that the signal can experience, due to several resonances in the input matching network. Moreover, it requires moderate to large silicon area and introduces high insertion loss at input network due to limited quality factor of inductors and degrades the amplifier noise figure (NF). Reference [23] shows improvement the operation of UWB receiver by compensation method and using pre-filter, significantly. Also, we have restriction in using additional filter.

Another method for increasing the bandwidth of a narrow band amplifier for UWB application is feedback solution. The feedback network could be inductive [15], resistive [16] or parallel resistive-capacitive [17]. The feedback could widen the bandwidth of LNA and improves the stability especially at high frequency. Furthermore, the precise design with double feedback network could give advantage of matching circuit with less inductor at the input. We must mention that the on-chip inductor has low quality factor that could degrades the noise figure of LNA.

The proposed UWB CMOS LNA used from two feedback network, resistive and capacitive–resistive, as shown in Fig. 4. The main advantage in our circuit is the low power consumption that makes it suitable for portable devices. The low noise figure of the circuit at all UWB could be done without high current in first stage.

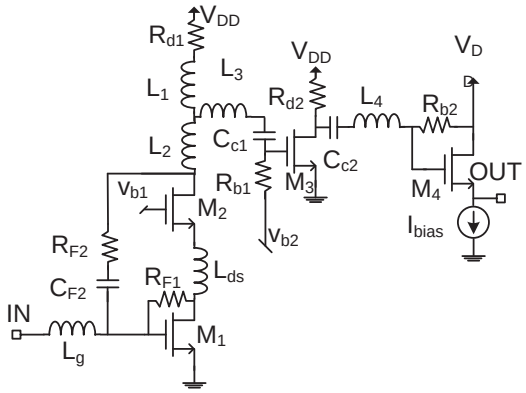


Fig. 4. Proposed UWB LNA

Double feedback with only one inductor at input transistor is used to have wideband input impedance matching. This simple impedance matching network could improve the power consumption and noise figure compare to the other UWB impedance matching topologies.

The π-section and T-section improve the power gain in cascode structure. The cascode topology is used to widen the bandwidth and provides good isolation of output from input. The power gain of this amplifier at higher frequencies is also degraded due to the capacitive effect of large size M_1 and M_2. To counterbalance this gain degradation, a series-peaking inductor L_2 as shown in Fig. 4 is added to make the

power gain improves at upper edge of UWB. The inductor L_2 could also resonate with C_{d2}. The C_{d2} is parasitic capacitor at drain of M_2. C_{d2} is parallel combination of gate-drain capacitor (C_{gd2}) and drain-bulk capacitor (C_{db2}) of M_2.

The LNA consists of two transistors as cascode (M_1, M_2), a gain stage (M_3) and a buffer stage (M_4). The inductor, L_g, beside gate-source capacitor of M_1 (C_{gs1}) and double feedback (R_{F1}, $C_{F2}R_{F2}$) are used for wide band input impedance matching and noise matching of the circuit. R_{d1} and L_1 make shunt peaking technique in drain of transistor M_2 that improves the bandwidth of LNA. The T-section inductor, L_1, L_2 and L_3 makes double series peaking technique to improve the gain and bandwidth. Also L_{ds} beside parasitic capacitor at drain of M_1 and source of M_2 makes a π-section that improves the bandwidth of LNA. The common source transistor (M_3) is used for improve the gain. The inductor L_4 resonate with C_{gs4} (gate-source capacitor of M_4) and C_{c2} to improve the bandwidth. Finally, the transistor M_4 is used to make a buffer stage for output impedance match up to 50Ω, standard resistor. In addition to the point of self-biasing of R_{F1}, the feedback resistors R_{F1} and $C_{F2}R_{F2}$ are also beneficial for the input impedance matching. Also, the feedback resistors R_{F1} and R_{F2} are used to have better input impedance matching over wide band and more stability.

4. Gain Analysis

In the output, the transistor M_4 is used as a buffer that also brings us output matching over ultra wideband frequency. The output impedance of the circuit could be written as (1).

$$Z_o \approx \frac{1}{g_{m4} + j\omega\left(C_{gs4} + C_{gb4}\right) + \frac{1}{Z_{bias}}} \qquad (1)$$

The g_{m4}, C_{gs4} and C_{gb4} are the transconductance, gate-source capacitor and gate-bulk capacitor of transistor M_4, respectively. Also Z_{bias} is impedance of I_{bias}. I_{bias} is made of a single transistor (M_5), so Z_{bias} is equal to $(1/jwC_{gd5})||(r_{ds5})$. C_{gd5} and r_{ds5} are gate-drain capacitor and drain-source resistor of transistor M_5 respectively. We could choose appropriate M_4 dimension to have output impedance matching. The buffer voltage gain can be written as (2):

$$\frac{v_o}{v_{g4}} \approx \frac{Z_L\left(g_{m4} + j\omega\left(C_{gs4} + C_{gb4}\right)\right)}{Z_L\left(g_{m4} + j\omega\left(C_{gs4} + C_{gb4}\right)\right) + 1} \qquad (2)$$

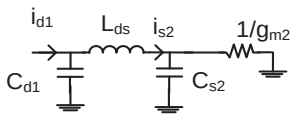


Fig. 5. broadband π-section between Transistors M_1 and M_2

In (2), Z_L is the standard impedance (50Ω) parallel with r_{ds4} and Z_{bias}. The value of r_{ds4} and Z_{bias} is much greater than Z_L. Also the capacitor of gate-source (C_{gs4}) is in femtofarad range, so in UWB frequencies the buffer voltage gain is about 0.5.

Middle stage with transistor M_3 is used for gain and bandwidth improvement and its effect on the gain of the circuit is very crucial. Voltage gain from gate of transistor M_3 to gate of transistor M_4 is shown in (3).

$$\frac{v_{g4}}{v_{g3}} = \frac{-g_{m3}\left(R_{d2}\left(Z_L - j\frac{1+Z_L g_{m4}}{\omega(C_{gs4}+C_{gb4})}\right)\right)}{R_{d2} + Z_L + j\left(\omega L_4 - \frac{1+Z_L g_{m4}}{\omega(C_{gs4}+C_{gb4})}\right)} \qquad (3)$$

In (3), g_{m3} is the transconductance of transistor M_3. Series peaking is used to improve the bandwidth. Inductor L_4 resonates with capacitor $(C_{gs4}+C_{gb4})/(1+g_{m4}Z_L)$.

The next gain is v_{g3}/v_{d2}, that could be derived as (4). In (4), Z_{ib} is input impedance of gain-stage (M_3) and is about to $1/(j\omega C_{g3})=1/[j\omega(C_{gs3}+C_{gb3}+(1+A)C_{gd3})]$. C_{g3} and C_{gd3} are total capacitor at gate and capacitor of gate-drain of transistor M_3. The A is voltage gain between drain to gate of transistor M_3.

Equation (4) shows a shunt peaking technique. The gain roll-off is compensated by R_{d1} and L_1. Moreover, it shows double series peaking technique that C_{g3} makes two spurious resonances with inductors L_{eff} and L_2+L_3, respectively. L_{eff} is $(L_1L_2+L_2L_3+L_1L_3)/(L_1+L_2)$. In the other word we use triple series peaking technique to increase the bandwidth of the amplifier and improve the power gain.

The current that flows from the M_1 should transfer to output. For calculation the i_{s2}/i_{d1} we must see the parasitic capacitor at the drain of M_1 (C_{d1}) and source of M_2(C_{s2}). i_{s2} and i_{d1} are source current of transistor M_2 and drain current of transistor M_1, respectively. Parasitic capacitor C_{s2} is parallel combination of C_{gs2} and C_{sb2}. C_{gs2} and C_{sb2} are source-gate and source-bulk capacitor of transistor M_2, respectively. Also, C_{d1} is parallel combination of C_{gd1} and C_{db1}. C_{gd1} and C_{db1} are gate-drain and drain-bulk capacitor of transistor M_1, respectively. C_{d1} and C_{s2} provides additional path for current signal to the ground and degrade the broadband performance of the LNA. L_{ds}, C_{d1} and C_{s2} form a broadband π-section LC network as Fig.5.

$$\frac{v_{g3}}{v_{d2}} = \frac{R_{d1} + j\omega L_1}{R_{d1}\left[1 - \omega^2 C_{g3}(L_2 + L_3)\right] + j\omega\left[L_2 + L_1 - \omega^2 C_{g3}(L_1L_2 + L_2L_3 + L_1L_3)\right]} \qquad (4)$$

In another word, for improvement in power gain and bandwidth, inductor L_{ds} is added between the drain of M_1 and source of M_2. With precise design, L_{ds}, C_{s2} and C_{d1} will resonate in lower edge frequency of desire band [18]. Equation (5) shows the relation between i_{s2} and i_{d1}:

$$\frac{i_{s2}}{i_{d1}} = \frac{(j\omega C_{s2} + g_{m2})/(C_{d1} + C_{s2})}{j\omega[1 - \omega^2 L_{ds}(C_{d1}||C_{s2})] + \frac{g_{m2}}{C_{d1}+C_{s2}}[1 - \omega^2 L_{ds} C_{d1}]} \quad (5)$$

In (5), g_{m2} is the transconductance of transistor M_2. To derive the transconductance of the first stage, (i_{d1}/v_{gs1}), we must notice that the input network impedance is about to R_s over the wide bandwidth. Feedback resistors (R_{F1} and R_{F2}) bring us more bandwidth and wideband matching against the frequencies of 3.1GHz to 10.6GHz.

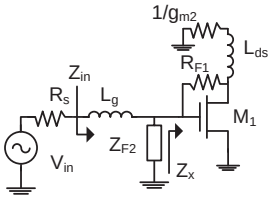


Fig. 6. Equivalent circuit at input stage

We can write the relation between drain current of transistor M_1 and input voltage source with regard to Fig.6 and pretty large value of R_{F1} and R_{F2}. We must mention that $Z_{F2}=R_{F2}/(1-A_{vc})$, which A_{vc} is the voltage gain between gate of M_1 and drain of M_2. After some calculation we would have:

$$\frac{i_{d1}}{v_{in}} \approx g_{m1}\frac{(Z_x||Z_{F2})}{(Z_x||Z_{F2}) + sL_{g1} + R_s} \quad (6)$$

In (6) Z_x is the input impedance form gate of M_1. Z_x could be written as (7):

$$Z_x = \frac{1}{j\omega(C_{gb1} + C_{gs1})}||\left(\frac{1 + g_{m2}R_{F1}}{g_{m2} + g_{m1}}||\frac{1}{j\omega\frac{g_{m1}L_{ds}}{R_{F1}+g_{m2}}} + \frac{1}{g_{m1}}||j\omega\frac{g_{m2}}{g_{m1}}L_{ds}\right) \approx \frac{1}{j\omega(C_{gb1} + C_{gs1})}||\frac{R_{F1}}{1+\frac{g_{m1}}{g_{m2}}} \quad (7)$$

From (6) and (7) we could write the input impedance of the circuit as (8):

$$Z_{in} = j\omega L_g + Z_{F2}||\frac{R_{F1}}{1 + g_{m1}/g_{m2}}||\frac{1}{j\omega C_{gs1}} \quad (8)$$

The Quality factor of the circuit shown in Fig. 7 can be approximately given by (9):

$$Q \approx \frac{\omega L_g}{R_s + \frac{\mathrm{Re}(Z_{F2})||\frac{R_{F1}}{1+g_{m1}/g_{m2}}}{\left[\left(\mathrm{Re}(Z_{F2})||\frac{R_{F1}}{1+g_{m1}/g_{m2}}\right)(\mathrm{Im}(Z_{F2})+\omega C_{gs1})\right]^2+1}} \quad (9)$$

From (9), and considering the inversely linear relation between the bandwidth and the quality factor, the narrowband LNA can be converted into a ultra wideband amplifier by the proper selection of feedback network. The feedback resistors also provide its conventional roles of flattening the gain over a wider bandwidth with much smaller noise figure degradation. Depending on the required bandwidth and noise contribution, the feedback resistor is chosen. Also smaller feedback resistor makes smaller quality factor and more bandwidth and better input impedance matching as (8). Although noise calculations will show us inverse relation between noise figure and the value of feedback resistors, we need compromise between noise and gain with input return loss and bandwidth.

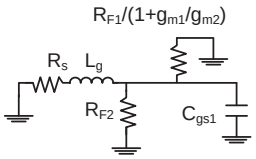


Fig. 7. Equivalent circuit for Q-factor calculation

5. Noise Analysis

The main source of noise that increases the noise figure of a circuit is the first stage. So, to have a glance at noise figure of a circuit, we could analysis the noise of the first stage. In this section we analyze the noise figure of resistive shunt feedback in the first stage of CS LNA (Fig. 4) for three main sources of noise in this structure. To simplify the calculations, transistor is assumed to have infinite output impedance. Beside the thermal noise of R_{F1}, R_{F2} (shunt feedback resistors), the drain noise current, due to the carrier thermal agitation in the channel and the induced gate noise, because of the coupling of the fluctuating channel charge into the gate terminal are taken into account.

The induced gate noise, drain noise and resistor noise power spectral densities are formulated as follows, respectively [13].

$$S_{i_{ng}} = 4kT\delta\frac{\omega^2 C_{gs}}{5g_{d0}} \quad (10)$$

$$S_{i_{nd}} = 4kT\gamma g_{d0} \quad (11)$$

$$S_{i_{nF}} = 4kT/R_F \quad (12)$$

Where δ, γ are technology dependent and g_{d0} is the channel conductance at $V_{DS}=0$. Also, T and K are temperature and Boltzmann constant, respectively.

Three noise sources, shown in Fig.8(a), are input referred in a conventional way and replaced by two correlated noise generators, as are shown in Fig.8(b):

$$i_n = \frac{R_F\left(g_m + j\omega C_{gs}\right)}{g_m R_F - 1} i_{nF} + \frac{1 + jR_F\omega C_{gs}}{g_m R_F - 1} i_{nd} + i_{ng} \quad (13)$$

$$e_n = \frac{1}{g_m} i_{nF} + \frac{1}{g_m} i_{nd} \quad (14)$$

(a) (b)

Fig. 8. (a) Three main noise source (b) Classic input referred noise as e_n and i_n

By the notification of the operation frequency (UWB) and small amount of gate-source capacitor and pretty big R_F, we can rewrite i_n as (15). Pretty large feedback resistor helps us reduce the noise effect of it on the noise figure of circuit as we would see in forward equations of noise calculations.

$$i_n = i_{nF} + j\left(\frac{\omega}{\omega_T}\right) i_{nd} + i_{ng} \quad (15)$$

Where $\omega_T = g_m/C_{gs}$ is the unity gain frequency. We can model the noise due to thermal noise of input voltage source resistor R_s as $v_{ns}(t)$. So if the noise power spectral density (PSD) due to $v_{ns}(t)$ be represented as $S_{v_{ns}} = 4KTR_s$, the noise figure (NF) of first stage is given by (16):

$$NF = 1 + \frac{S_{e_n} + S_{i_n}}{S_{v_{ns}}} \quad (16)$$

In (16), S_{e_n} and S_{i_n} are the input referred noise PSDs due to the internal noise source of M_1 and resistor R_F. A simple expression for the input referred noise current power spectral density (PSD) is given by:

$$\frac{S_{i_n}}{4KT} = G_F + \frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)^2 g_m(1 + \chi^2\alpha^2 + 2|c|\alpha\chi) \quad (17)$$

Where $\chi = \sqrt{\delta/(5\gamma)}$, and $c = S_{i_{ng}i_{nd}}/\sqrt{S_{i_{ng}}S_{i_{nd}}}$ is the correlation coefficient between the gate noise and the drain noise for MOS device, is $c \approx j0.395$ [19]. We must notice that there is no correlation between the noise of resistor R_F and gate noise and drain noise. The parameter $\alpha = g_m/g_{d0}$ accounts for short channel effect. It describes the transconductance reduction due to velocity saturation and mobility decrease due to vertical fields [13].

Calculations of the input referred noise voltage power spectral density (PSD) are carried out as (18):

$$\frac{S_{e_n}}{4KT} \approx \left(\frac{1}{\alpha g_m}\right)\left(\frac{\alpha}{R_F g_m} + \gamma\right) \quad (18)$$

The noise voltage can be expressed as the sum of two components, one fully correlated, e_{nc}, and the other, e_{nu}, uncorrelated to the noise current as (19):

$$e_n = e_{nc} + e_{nu} \quad (19)$$

Carrying out the calculations, the correlation impedance Z_c, is written as (20):

$$Z_c = \frac{e_{nc}}{i_n} = \frac{\overline{e_{nc}.i_n^*}}{\overline{i_n.i_n^*}} = \frac{\overline{(e_{nc} + e_{nu}).i_n^*}}{\overline{i_n.i_n^*}} = \frac{S_{e_n i_n}}{S_{i_n}} = R_c + jX_c \quad (20)$$

$$R_c = \frac{G_F/g_m}{G_F + \frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)^2 g_m(1 + \chi^2\alpha^2 + 2|c|\alpha\chi)} \quad (21)$$

$$X_c = -\frac{\left(\frac{\omega}{\omega_T}\right)\frac{\gamma}{\alpha} g_m(|c|\alpha\chi + 1)}{G_F + \frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)^2 g_m(1 + \chi^2\alpha^2 + 2|c|\alpha\chi)} \quad (22)$$

G_F is $1/R_F$ in (21) and (22). If the R_F was pretty large the real part of Z_c is about zero in compare with X_c.

The two uncorrelated noise source, e_{nu} and i_n, are described by means of the following parameters, respectively:

$$R_u = \frac{S_{e_{nu}}}{4KT} = \frac{1}{4KT}\frac{S_{i_n}S_{e_n} - |S_{i_n e_n}|^2}{S_{i_n}} \quad (23)$$

$$G_n = \frac{S_{i_n}}{4KT} \quad (24)$$

By using the introduced parameters, the NF can be expressed as follows [13]

$$NF = 1 + \frac{R_u + G_n|Z_c + Z_s|^2}{R_s} = 1 + \frac{R_u + G_n[(R_c + R_s)^2 + (X_c + X_s)^2]}{R_s} \quad (25)$$

Here $Z_s = R_s + jX_s$ is the source impedance. Classic noise optimization theory shows that the minimum noise figure is achieved if the source impedance $Z_s = Z_{opt} = R_{opt} + jX_{opt}$ could be chosen such as it is in [7].

$$R_{opt} = \sqrt{\frac{R_u}{G_n} + R_c^2} \approx \sqrt{\frac{R_u}{G_n}} \quad (26)$$

$$X_{opt} = -X_c \quad (27)$$

With the notification of equations (23) to (27) the noise figure can be rewritten as (28):

$$NF_{min} = 1 + 2\left[Re\left(S_{e_n i_n}\right) + \sqrt{S_{e_n}S_{i_n} - \left(Im\left(S_{e_n i_n}\right)\right)^2}\right] \quad (28)$$

Where Re() and Im() means real and imaginary parts of equation. In this situation that $S_{e_n i_n}$ just have imaginary part we can rewrite the (28) as (29).

$$NF_{min} = 1 + 2\sqrt{S_{e_n}S_{i_n} - |S_{e_n i_n}|^2} \quad (29)$$

The minimum noise figure (NF_{min}) can be written by (30) Where the $B_1(\omega)$ and $B_2(\omega)$ are as (31) and (32).

$$NF = 1 + 2\sqrt{G_F . B_1(\omega) + B_2(\omega)} \quad (30)$$

$$B_1(\omega) = \frac{\gamma}{\alpha g_m}\left\{1 + \left(\frac{\omega}{\omega_T}\right)^2 (1 + \chi^2\alpha^2 + 2|c|\alpha\chi)\right\} \quad (31)$$

$$B_2(\omega) = \left(\frac{\omega}{\omega_T}\right)^2 \gamma^2\chi^2(1 - |c|^2) \quad (32)$$

At first glance at (30), shunt feedback will degrade the minimum noise figure (NF_{min}), but if R_F be pretty large, it has not very bad effect on noise figure, especially it is divided on g_m of transistor.

The total noise figure (NF) can be written by minimum noise figure (NF_{min}) and other parameters [13] as (33):

$$NF = NF_{min} += 1 + \frac{G_n}{R_s}\left[(R_s - R_{opt})^2 + (X_s - X_{opt})^2\right] \quad (33)$$

The total noise figure (NF) will be more than (33) due to finite quality factor of the inductors that are used at the input of the transistors, the channel and gate noise of transistor M_2 and M_3 and resistor R_{d1} and R_{d2}. The contribution of transistor M_2, M_3 and M_4 in noise is much smaller than M_1. For reducing the noise of the input inductor we must use inductor with high quality factor.

6. Circuit Design and Simulation

The layout of the finished circuit is shown in Fig. 9. The layout area is 1.058 × 0.658 mm^2 excluding the test pads.

The design, simulation, post layout simulation and Trimming of the proposed CMOS UWB LNA, are based on the TSMC 0.18µm RFCMOS process. For better performance at high frequencies and lower parasitic, a minimum channel length of 180nm is chosen for all the transistors in the circuit.

The power budget of the circuit for low power designing is chosen about 10mW. So the current budget is about 6mA from 1.8V voltage supply. The width of M_1 transistor (192µm) is optimized for noise. The M_1 width is sized, for 4mA current, so that the contributions of thermal and induced gate noise and impedance matching are balanced

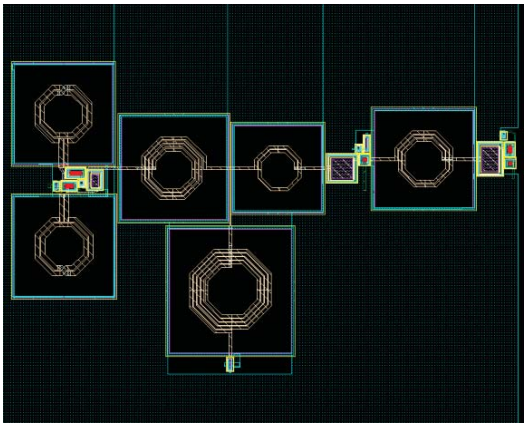


Fig. 9. Photograph of the Layout of proposed LNA

. The width of M_2 transistor (288µm) is decided considering a trade-off between gain and bandwidth. Although the feedback resistor R_{F1}= 1700Ω and R_{F2} = 500Ω are optimal from the simulation results due to the respectable noise performance. The value of R_{F1} and R_{F2} are adjusted as 1870Ω and 411Ω, respectivelyin order to guarantee reasonable wideband input matching.

The R_{d1} and L_1 are designed to achieve flat gain over the whole bandwidth and make a roll-off factor at appropriate frequency. The value of L_1 is designed by two opposite requirements. It must be sizable to have large gain and it must be small so that it resonates with L_3 and C_{gs3}, out-of-band, as well. R_{d1} is chosen to place the zero frequency as close as possible to the lower edge of the band to improve the gain at lower frequencies. An upper limit to R_{d1} is set by the voltage headroom. The values for the components of the load are: R_{d1} = 134Ω and L_1 = 4.04nH.

The narrowband LNA is designed at 7 GHz. By the proper selection of the values for L_g, with feedback resistors, R_{F1} and R_{F2}, the bandwidth extends to cover 3.1–10.6GHz. L_g for in band matching is selected as 595 pH.

The value of L_2 is chosen to be 582pH for resonating and peaking with parasitic capacitor at drain of M_2 (C_{d2}) at the frequency of 10GHz as mentioned before.

The inductor L_3 at T-section makes series peaking with input capacitor from M_3 transistor (C_{gs3}) has the value 1.96nH to smooth the gain at high frequency.

Proper choose of inductor L_{ds} can resonate with the parasitic capacitor at drain of M_1 (C_{d1}) and resonates out of band in series with capacitor at source of M_2 and drain of M_1, ($C_{d1}||C_{s2}$) to show a broadband property. It is chosen in this design as 582pH.

Second stage with 2.5mA current usage is designed to improve the overall gain of the circuit. The width of transistor M_3 is chosen to 80µm. Drain resistor (R_{d2}) is chosen 200Ω to make reasonable gain for LNA. The inductor L_4 has the value of 1.15nH to resonate with capacitor C_{c2} and parasitic capacitor at gate of M_4(C_{gs4}) to improve the bandwidth of the circuit.

The buffer must drive a 50Ω external load and is used for measurements and output impedance matching. The buffer is biased by means of a current source made up of one transistor. The bias current for this stage is selected due to has proper output return loss although it reduces the power gain. The current about 2.4mA is chosen for buffer stage.

All design parameters are listed in Table 1. Post layout simulation shows the dc current of first stage is about 3.7mA and 2.5mA for second stage. From the supply voltage of 1.8V, the power consumption of the 3.1-10.6GHz LNA is 11mW, without including the output buffer stage.

Fig. 10 and 11 show the effect of feedback networks (R_{F1}, R_{F2}) on noise figure of the circuit. As could be seen in Fig. 10 and 11 resistors feedback (R_{F1}, R_{F2}) directly improve the noise figure at all frequencies, as could be seen in (30).

Also Fig. 12 shows effects of R_{F2} on input return loss. Feedback resistor (R_{F2}) has inversely improved the S_{11}, as shown in Fig. 12. Equation (8) shows the same results.

Fig. 13 shows the power gain for three value of inductor L_1. We could see the inverse and direct relation between the value of inductor L_1 and power gain and bandwidth, respectively.

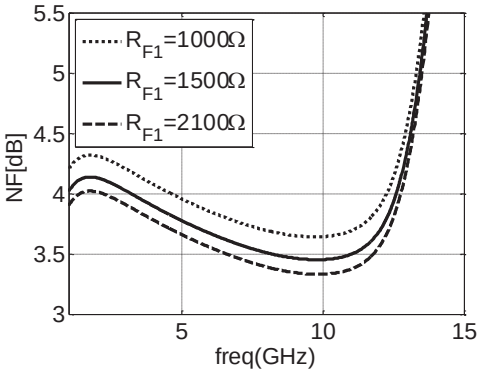


Fig. 10. Effect of variation of R_{F1} on NF of the LNA

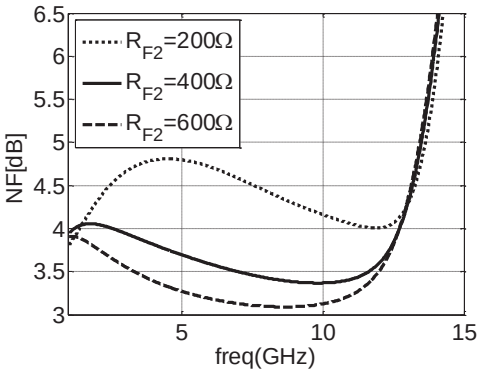


Fig. 11. Effect of variation of R_{F2} on NF of the LNA

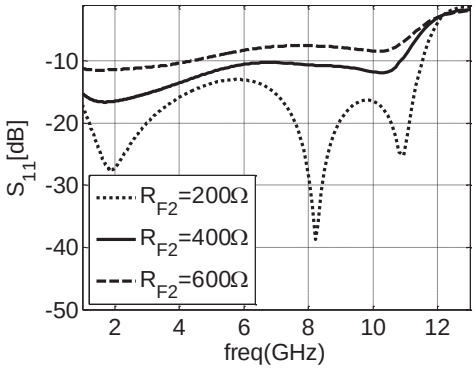


Fig. 12. Effect of variation of R_{F2} on S_{11} of the LNA

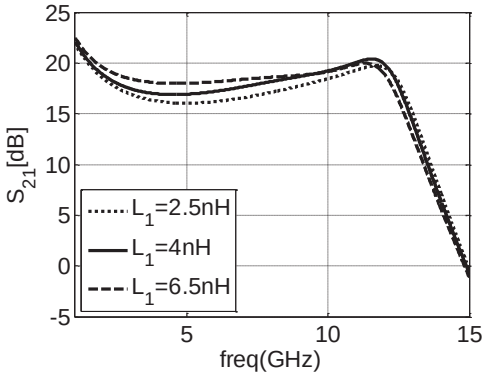


Fig. 13. Effect of variation of L_1 on S_{21} of the LNA

Equation (4) shows the same relations. Inductor L_1 in numerator of equation (4) has direct relation with power gain (S_{21}). On the other hand the inductor L_1 beside inductor L_3 resonates with C_{gs3} to improve the bandwidth, so choosing smaller value for L_1 makes higher resonance frequency and it improves bandwidth. So the optimum value of inductor L_1 could be chosen.

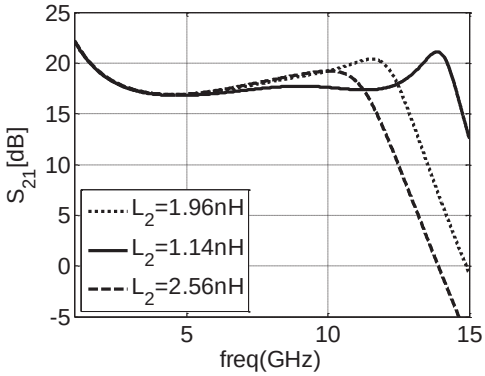


Fig. 14. Effect of variation of L_2 on S_{21} of the LNA

Fig. 14 shows the power gain for different value of inductor L_2. We could see the inverse relation between the value of inductor L_2 and bandwidth of the LNA. Equation (4) shows the same relation. The inductor L_2 resonates with C_{d2} to at edge of bandwidth to improve it, so choosing smaller value for L_1 makes higher

resonance frequency and it could improve the bandwidth.

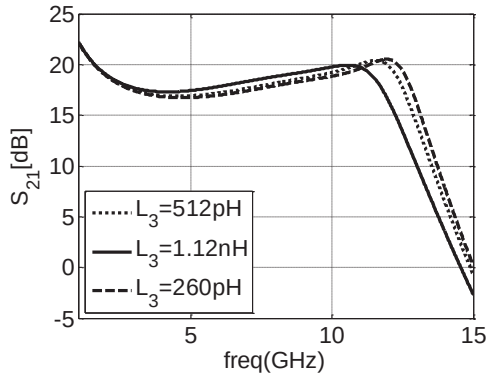


Fig. 15. Effect of variation of L_3 on S_{21} of the LNA

Fig. 15 shows the power gain (S_{21}) for three value of inductor L_3. We could see the inverse relation between the value of inductor L_1 and bandwidth. Equation (4) shows the same relation. Inductor L_3 resonates with C_{gs3} to improve the bandwidth, so choosing smaller value for L_1 makes higher resonance frequency and it improves the bandwidth.

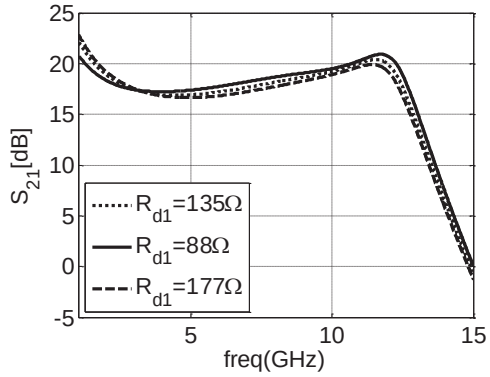


Fig. 16. Effect of variation of R_{d1} on S_{21} of the LNA

Fig. 16 shows the effect of R_{d1} on power gain (S_{21}) and could show the correctness of shunt peaking technique that is used by R_{d1} and L_1 at equation (4). Smaller R_{d1} makes roll-off factor is happen at smaller frequency. It could be seen at Fig. 16 that the power gain is falling for R_{d1}=88Ω, but it will rise at about 3.5 GHz due to shunt peaking. Shunt peaking is happen for R_{d1}=88Ω sooner, so its rising point is happen sooner compare with bigger R_{d1}. The rising point for bigger R_{d1} is happen later, at higher frequency, so for higher R_{d1} the power gain is smaller at high frequency.

Fig. 17 shows the effect of direct relation between feedback resistor and power gain. Equation (6) shows the same result. Also the bandwidth has inverse relation with feedback resistor as (9). So to select the feedback resistor we must consider the improvement of input return loss (as Fig.12) and power gain. On the other hand we must mention to noise figure. So the proper value of feedback resistor could be selected.

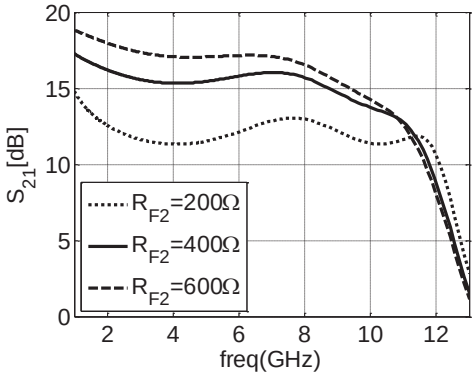


Fig. 17. Effect of variation of R_{F2} on S_{21} of the LNA

Fig. 18, 19, 20, 21, and 22 show the comparison between hand calculations and simulations of voltage gain (V_O/V_{G4}), (V_{G4}/V_{G3}), (V_{G3}/V_{D2}), (V_{D2}/V_{IN}) and NF (noise figure). We could see in Fig. 18 the same result of hand calculation and simulation result for voltage gain (V_O/V_{G4}). There are some differences between hand calculation and simulation in Fig. 19 and 20 in voltage gain (V_{G4}/V_{G3}) and (V_{G3}/V_{D2}). The reason for these differences is ignoring the parasitic resistance and capacitance of inductors in hand calculation, L_4 for Fig. 19 and L_1, L_2 and L_3 for Fig. 20, respectively. Hand calculation and simulation result are close to each other in Fig. 21 for voltage gain (V_{D2}/V_{IN}). Also, there are some differences especially at high frequencies due to ignoring parasitic resistance and capacitance of inductors L_{ds} and L_g in hand calculation. Also neglecting the gate-drain capacitance of M_1 has some effects in this different result.

The noise figure of first stage that used in hand calculation has some differences with simulation result due to noise of other transistors and resistors in other stages that was mentioned at the end of section 5.

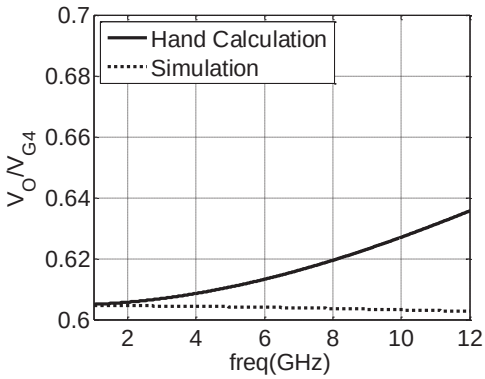


Fig. 18. Hand Calculation and Simulation of Voltage Gain V_O/V_{G4}

Fig.23 and 24 show the power gain and noise figure of CMOS UWB LNA over 3.1-10.6GHz, respectively. Noise figure (NF) is 3.6dB to 4.1dB and has ±0.25dB variations. Power gain is 15.6dB to 18.08dB was achieved over the 3.1-10.6GHz band of interest. Fig. 25 shows the post layout simulation of S_{12} against

frequency of the LNA that has the value less than -39 dB in full desire band. Fig. 26 and 27 show the post layout simulation of scattering parameters S_{11} and S_{22} against frequency of the CMOS UWB LNA, respectively. S_{11} is -9.6 to -13dB and S_{22} is -10.8 to -12.6dB, were achieved over the 3.1-10.6GHz band of interest.

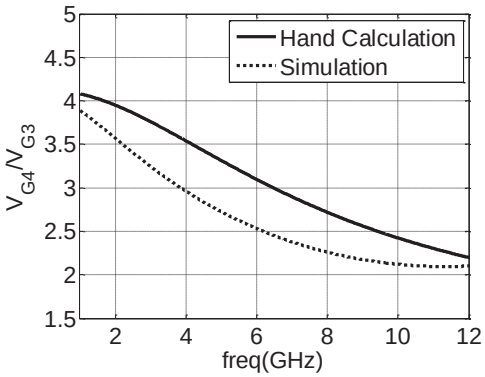


Fig. 19. Hand Calculation and Simulation of Voltage Gain V_{G4}/V_{G3}

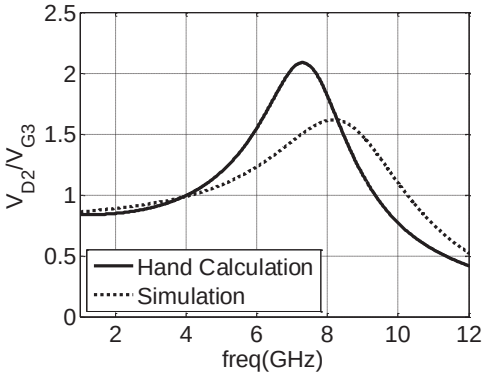


Fig. 20. Hand Calculation and Simulation of Voltage Gain V_{G3}/V_{D2}

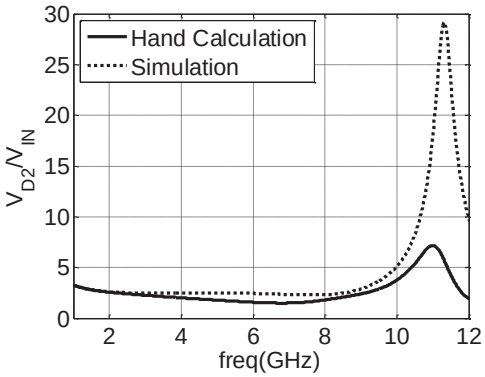


Fig. 21. Hand Calculation and Simulation of Voltage Gain V_{D2}/V_{IN}

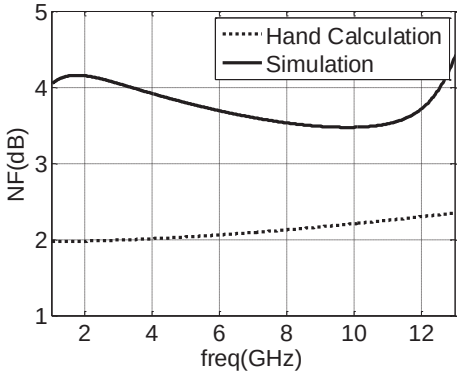


Fig. 22. Hand Calculation and Simulation of Noise Figure

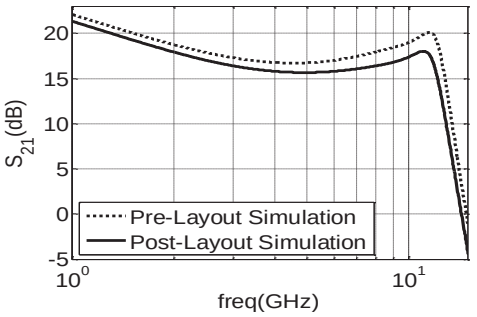


Fig. 23. Simulated Power Gain

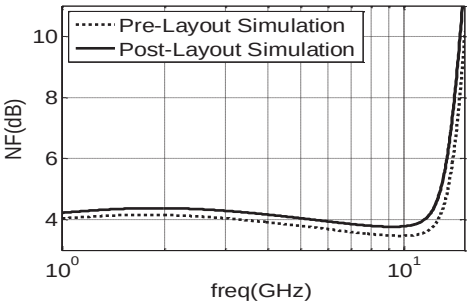


Fig. 24. Simulated Noise Figure (NF)

Fig. 28 shows the post layout simulation group delay against frequency characteristics of the CMOS UWB LNA. Simulation shows about 111±43ps of phase linearity for this circuit.

The two-tone test for third-order intermodulation distortion (IP3) is shown in Fig. 29. The test is performed at 4□GHz. Tone spacing is 1MHz. The simulated IIP3 is about -9.2dBm.

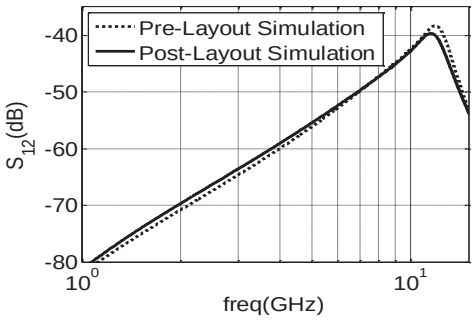


Fig. 25. Simulated reverse gain(dB)

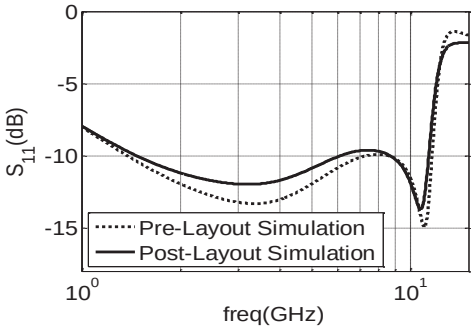


Fig. 26. Simulated input return loss(dB)

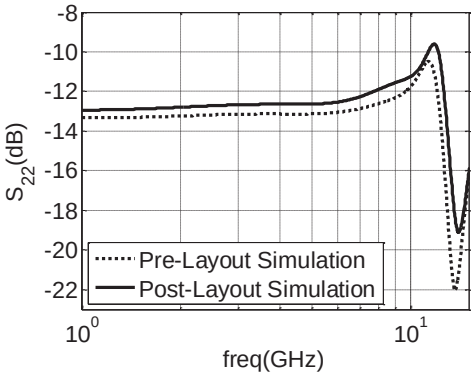


Fig. 27. Simulated output return loss(dB)

The IIP3 of the LNA was examined at seven different frequencies with 10 MHz frequency spacing at 4, 5, 6, 7, 8, 9, and 10GHz, respectively. As in Fig. 30 an average IIP3 is about -10dBm.

Simulation results of the proposed LNAs and the prior published state-of-the-art UWB LNAs are summarized in Table 1. For the comparison of different topologies, we include two figures of merit (FOMs) in the table 1, FOM I, which does not include voltage supply, and FOM II, which does:

$$FOM\ \mathrm{I} = \frac{S_{21}BW(GHz)}{(NF(abs\_min)-1)P_D(mW)} \qquad (34)$$

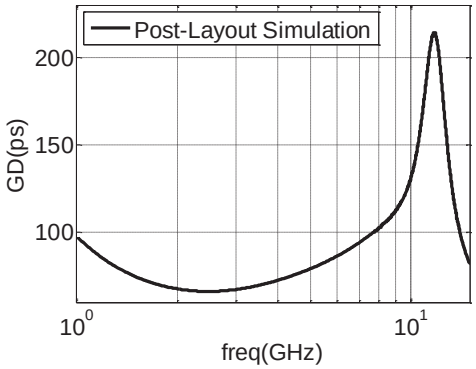


Fig. 28. Simulated Group Delay(ps)

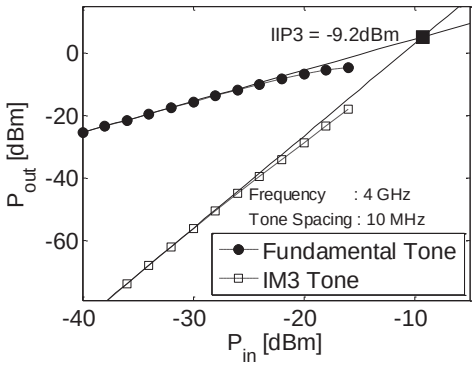


Fig. 29. Simulated IIP3 at 4 GHz

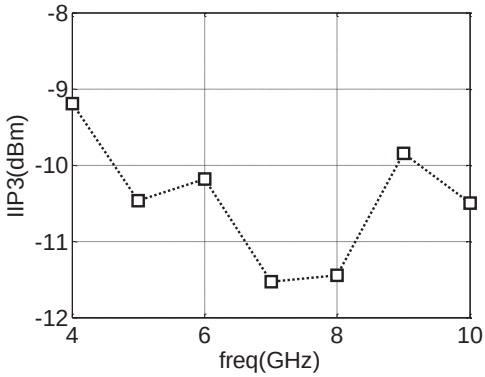
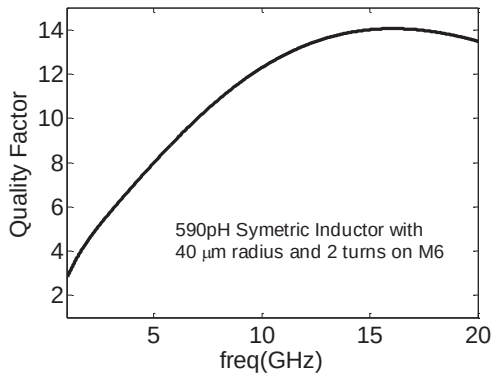


Fig. 30. Simulation IIP3 versus intermodulation frequency



$$FOM\ \text{II} = \frac{S_{21}BW(GHz)}{(NF(abs\_min)-1)P_D(mW)}\frac{1}{V_{DD}} \quad (35)$$

The table 1 shows one of the best FOM for this design with very good NF and excellent power gain, although the input return loss and power consumption of the proposed circuit are in good situation. The values of elements that are used in the proposed circuit are listed in table 2. The inductors L_g and L_{ds} are symmetric spiral inductor. The simulation shows 40 GHz self resonance frequency for inductor L_g. The quality factor of L_g is shown as Fig. 27 against frequency. The other inductors (L_1, L_2, L_3 and L_4) are chosen as standard spiral inductors. All of them have 9μm of width on metal 6 in TSMC 0.18 μm RF CMOS process. Types of capacitors that are used in the circuit are MIMCAP_rf capacitor. The type of resistors and transistors that are used in the design are listed in table 2. The post simulation results for extreme corner cases are shown in table 3.

Fig. 26. Quality factor of L_g (symmetrical inductor)

Table. 1. Performance Compared with the Fabricated Papers*

	This Work	**[4]**	**[6]**	**[7]**	**[8]**	**[15]**	**[17]**	**[20]**	**[21]**	**[22]**
Tech(nm)	**180**	180	180	180	180	90	180	180	180	180
BW(GHz)	**1-12.2**	0.1-11	2.8-10.4	2.2-9.5	2.3-10.5	0-14.5	3-10.6	1-12	3.2-11.5	3.1-9.8
S_{21}(dB)	**18.08**	8.1	10.4	10.1±1.1	14±1	10	13±0.5	9.5±1	14.8±1.2	9.5±1.5
S_{11}(dB)	**< -9.1**	<-12	<-11	<-10	<-10	<-10	<-9	<-12	<-8.3	<-10.5
NF (dB)	**3.6-4.1**	2.9	4.5-6	3.5-6.6	3-4	5.6-6	2.5-4.7	4.2-5	3-5.8	4.8-6
Power(mW)	**11.3**	21	2	8.9	17	30	14.1	20	11.7	4.6
IIP3(dBm)	**-9.2**	-3.4	-5.4	-9			-8	-6.2	-6.5	-7
FOM I(GHz/mW)	**6.3**	1.3	4.2	0.9	1.8	0.5	1.3	0.85	1.6	1.7
FOM II(GHz/VmW)	**3.5**	0.7	2.2	0.5	1	0.6	0.7	0.47	0.9	1

Table. 2. Device Value and Type of the proposed LNA

Transistor(W/L)	**Type**	**Resistor(Ω)**	**Type**	**Capacitor(pF)**	**Type**	**Inductor(nH)**	**Type**
M_1=24×8/0.18 μm/μm	rf2v	R_{b1} = 3830	rphripoly_rf	C_{c2} = 1.74	MIMcap_rf	L_1= 4.04	Standard
M_2=36×8/0.18 μm/μm	rf2v	R_{b2} = 4740	rphripoly_rf	C_{c1} = 1.84	MIMcap_rf	L_2= 1.96	Standard
M_3=10×8/0.18 μm/μm	rf2v	R_{F1} = 1870	rphpoly_rf	C_{F2} = 0.325	MIMcap_rf	L_3= .512	Standard
M_4=20×8/0.18 μm/μm	rf2v	R_{F2} = 411	rphpoly_rf			L_4= 1.15	Standard
		R_{d1} = 134	rplpoly_rf			L_g = 0.595	Symmetric
		R_{d2} = 200	rplpoly_rf			L_{ds} = 0.582	Symmetric

Table. 3. LNA's Performance on Extreme Corner Cases

	NF(dB)	**S21(dB)**	**S11(dB)**	**S22(dB)**	**Pdc(mW)**
SS , 90	4.4	16.4	-9	-11.3	11.9
SS , -40	3.1	17.9	-8.3	-9.9	11.7
SF , 90	4.4	17	-10.5	-11	14
SF , -40	3.8	17	-9	-8.5	12.6
FS , 90	4.3	19.4	-9.6	-8.1	12.4
FS , -40	2.8	19.8	-9.1	-12.5	14
FF , 90	4	19	-10.4	-8.5	14
FF , -40	3	19.5	-8.7	-10.3	14.2

7. Conclusion

This paper presented a new topology for low noise amplifier architecture that is operating in 3.1-10.6 GHz UWB range. The circuit design and post layout simulation were done with TSMC 0.18μm RF CMOS process. By utilizing special inductive peaking technique the gain and its flatness was improved. Using one inductor and double feedback at the input network enhanced the input impedance and noise matching in whole frequency band.

The design base on an optimization over the effective operating frequency band, noise figure and power consumption. The effective additional noise from feedback resistors is negligible due to the pretty large of the resistors. Noise calculation is done through a detailed noise analysis. Improvement in power gain was achieved by a shunt and series peaking technique and mixed π-section and T-section in the circuit. Post layout Simulation results show a flat noise figure of 3.85±0.25dB over the full UWB, power gain of 18.08 dB with bandwidth from DC to 12.2GHz. The linearity of the LNA was detected by IIP3 of -9.2dBm, while consuming 11.3mW from a 1.8V voltage supply. The layout area is about 0.696mm^2 excluding the test pads The excellent FOM of this work comparing to other works shows the advantage of the circuit for using in front-end of a multi-standard wireless system and portable devices.

References

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